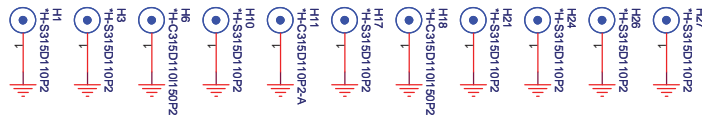
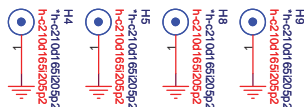


### ***M/B Screw Holes***

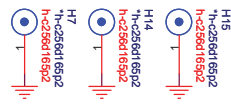
### M/B Screw Holes



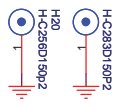
## CPU Bracket



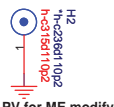
## VGA Bracket



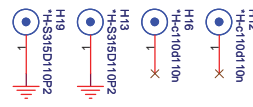
## TV Screw Holes



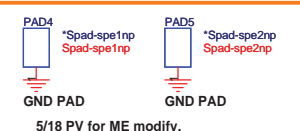
## BAT Screw Holes



### ODD Screw Holes



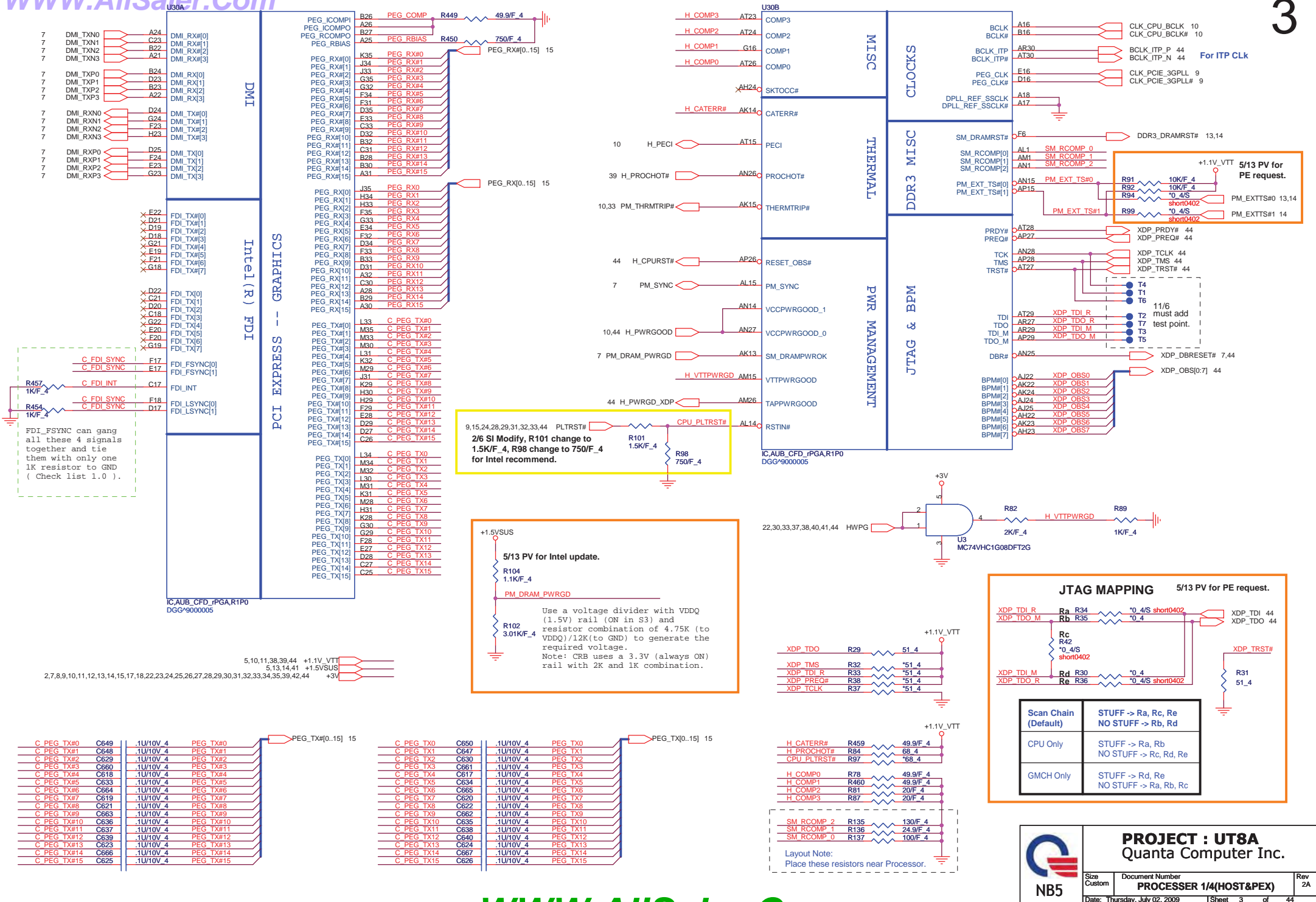
## EMI Spring PAD



**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>Clock Gen/Screw Holes</b>	Rev 2A
Date: Thursday, July 02, 2009		Sheet 2 of 44

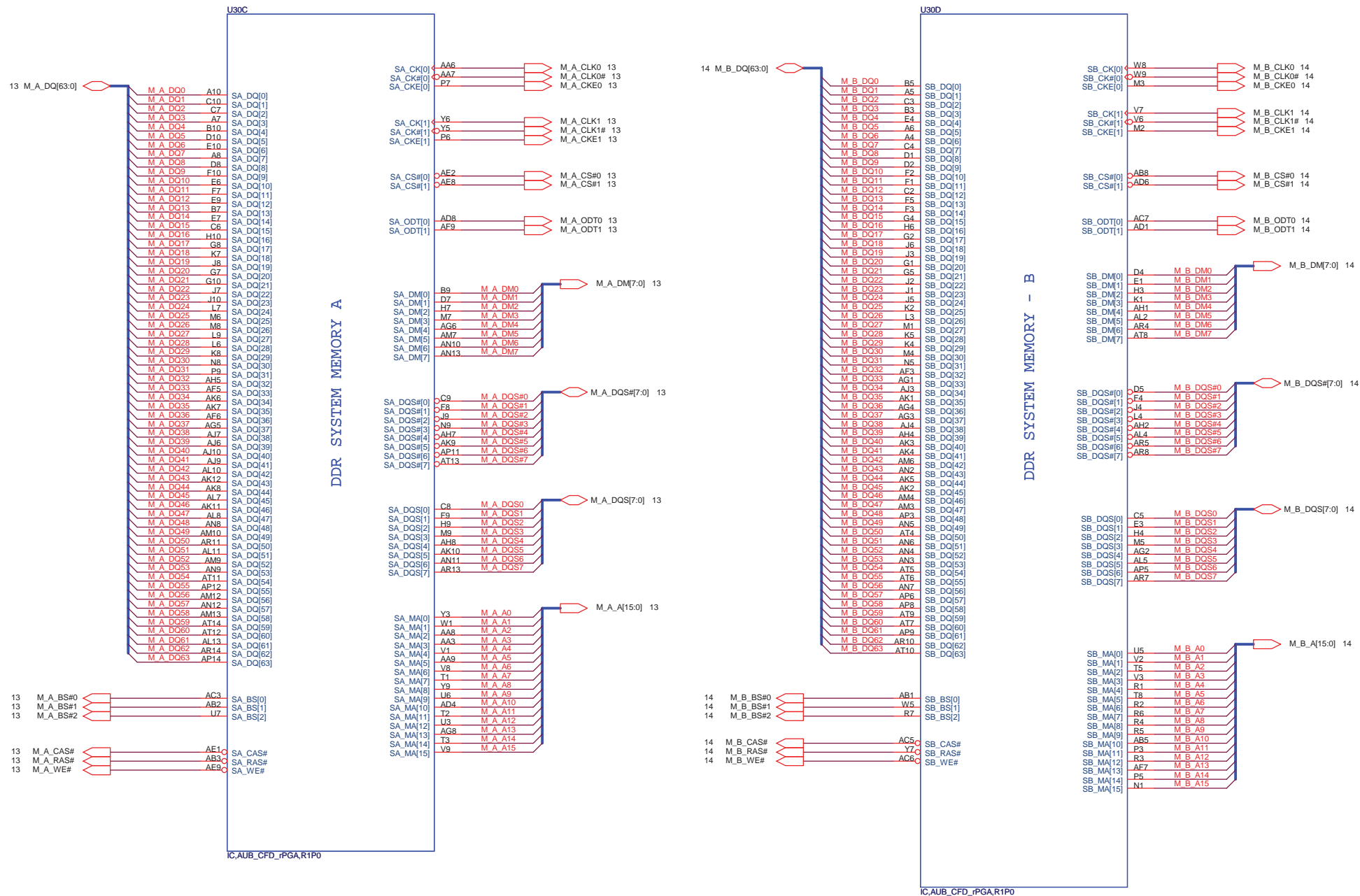




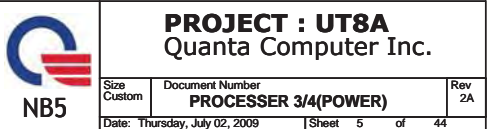


## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

4



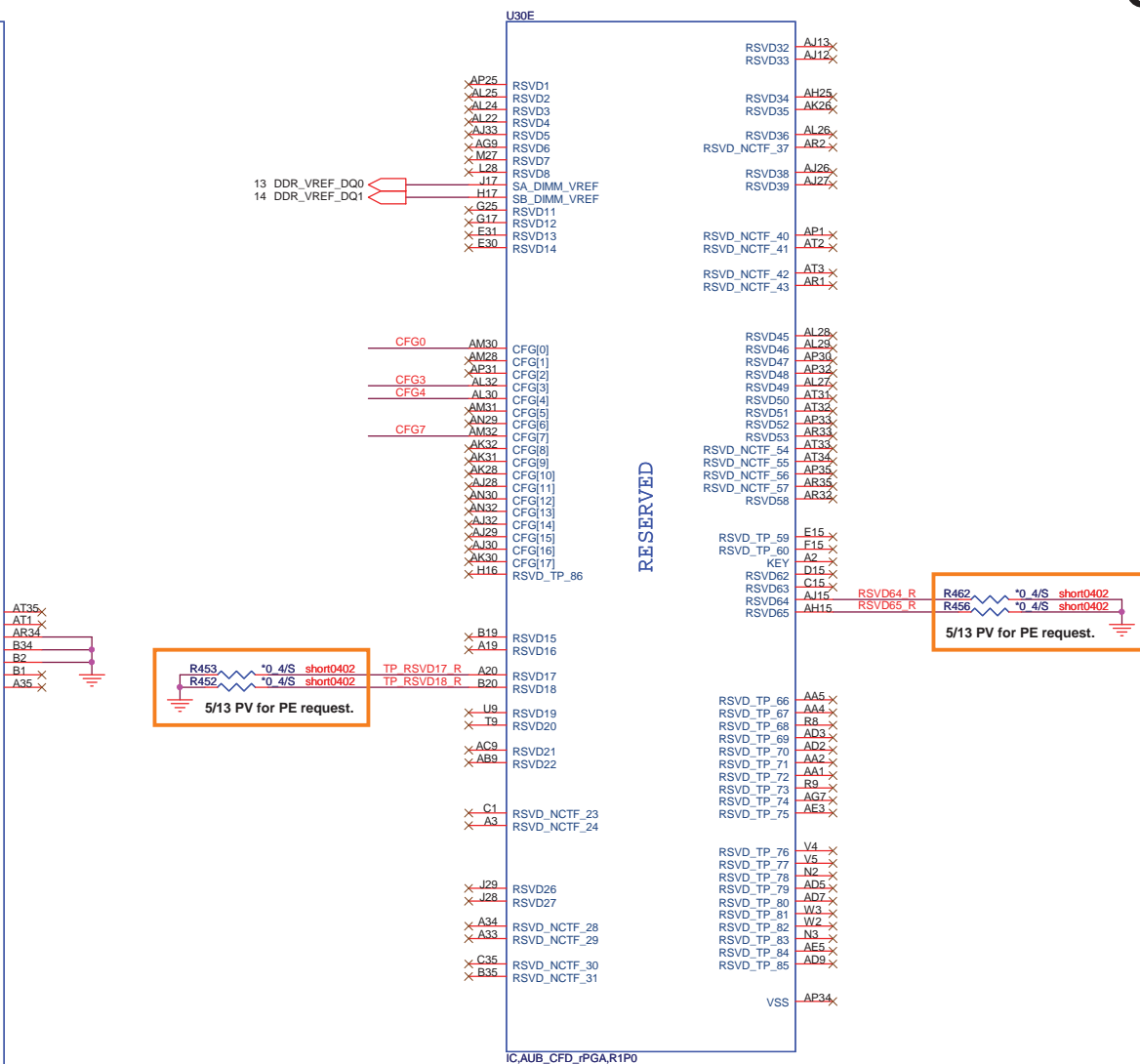
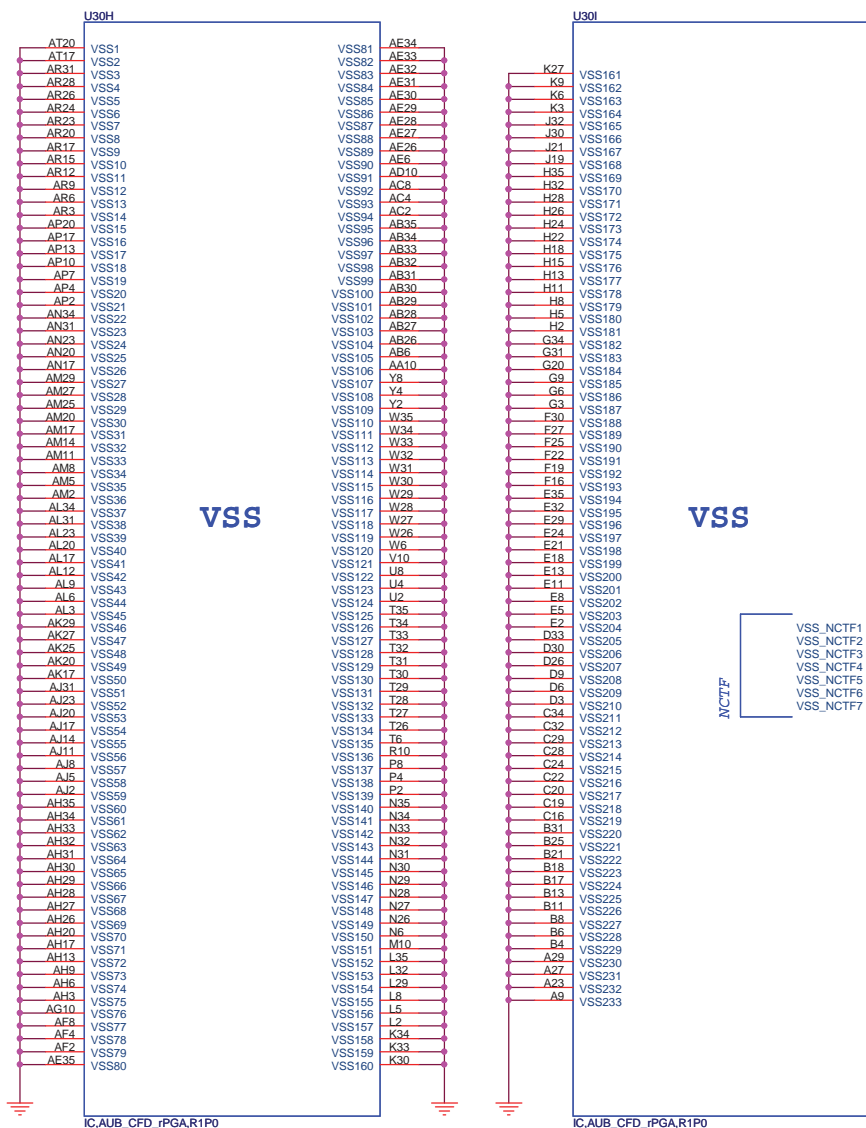




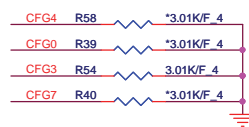


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

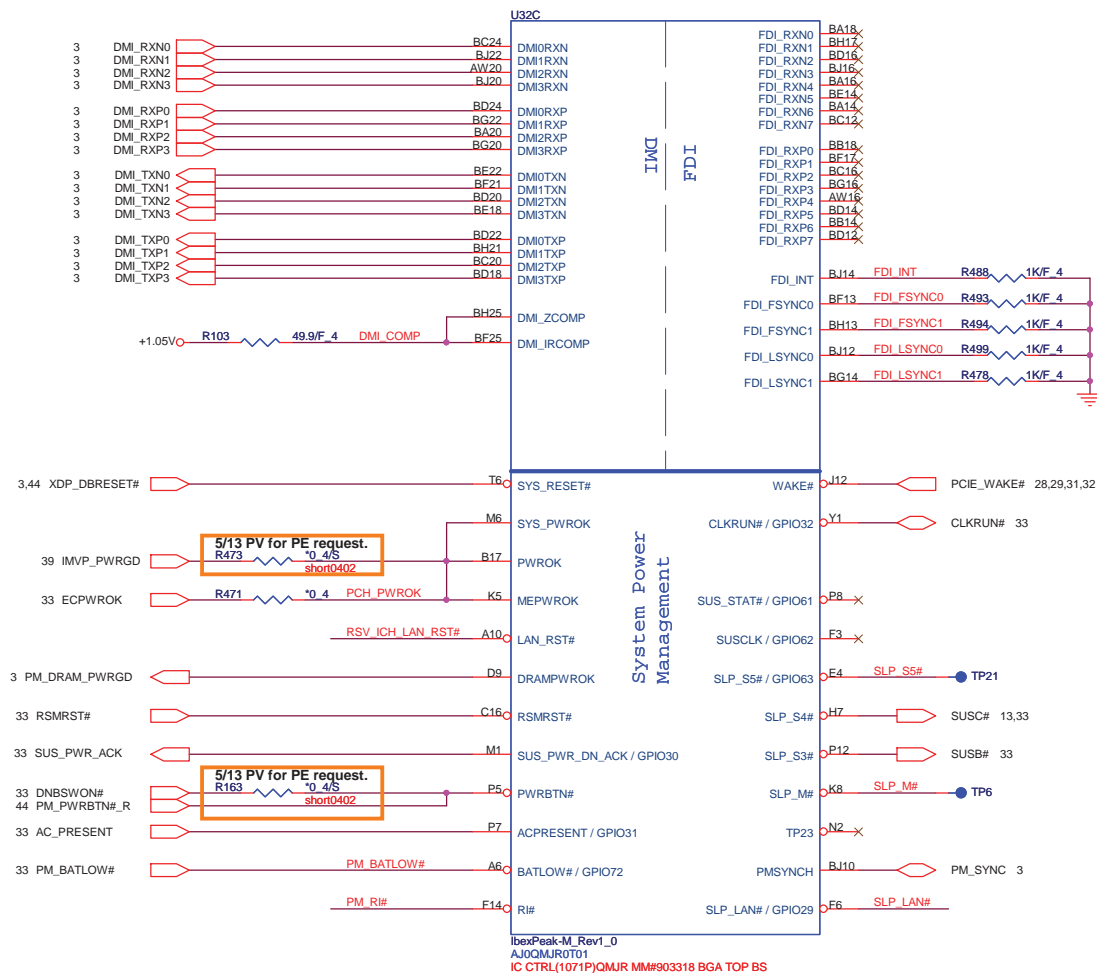
CFG[ 1:0 ] - PCI\_Epress Configuration Select  
 \*11= 1 x 16 PEG  
 \*10= 2 x 8 PEG

**PROJECT : UT8A**  
Quanta Computer Inc.

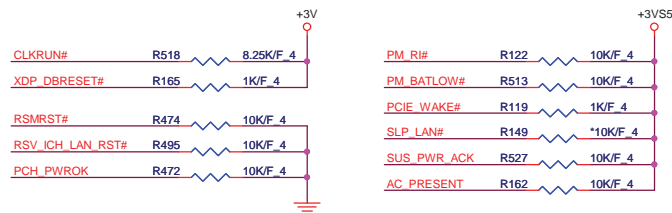
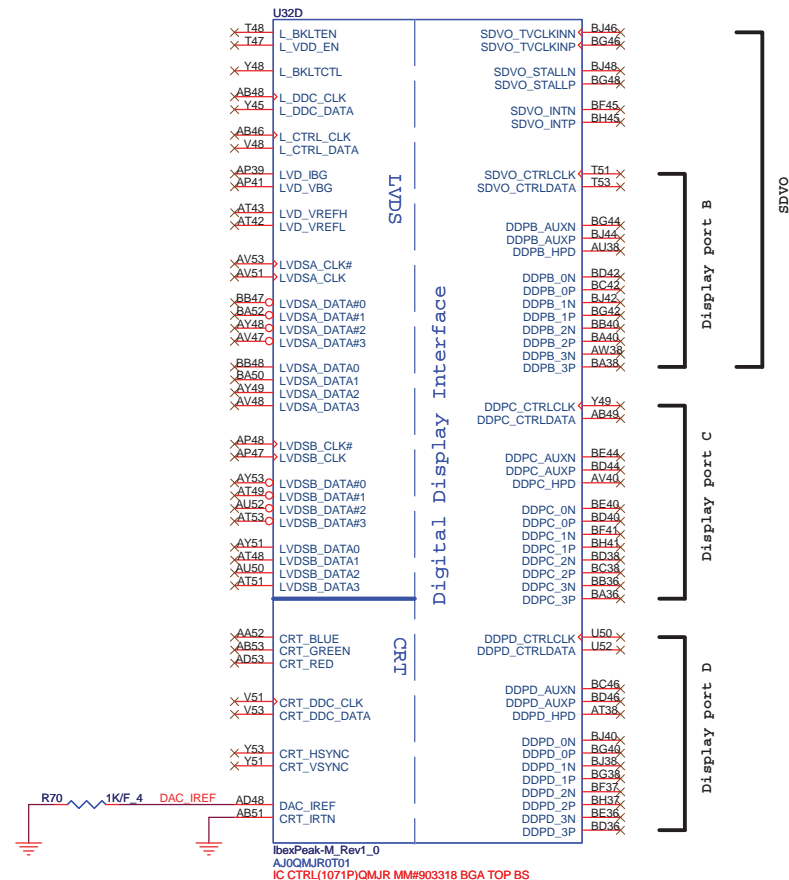
Size Custom	Document Number <b>PROCESSOR 4/4(GND)</b>	Rev 2A
Date: Thursday, July 02, 2009	Sheet 6 of 44	



# IBEX PEAK-M (DMI, FDI, GPIO)



# IBEX PEAK-M (LVDS, DDI)

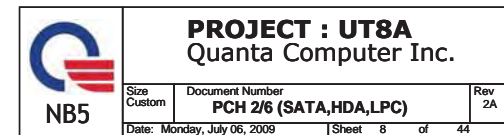


2,8,9,11,15,16,17,29,33,38,44 +1.05V  
2,3,8,9,10,11,12,13,14,15,17,18,22,23,24,25,26,27,28,29,30,31,32,33,34,35,39,42,44 +3V  
9,10,11,31,42,44 +3V5

**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>PCH 1/6 (DMI, PM, VIDEO)</b>	Rev 2A
Date: Thursday, July 02, 2009	Sheet 7 of 44	

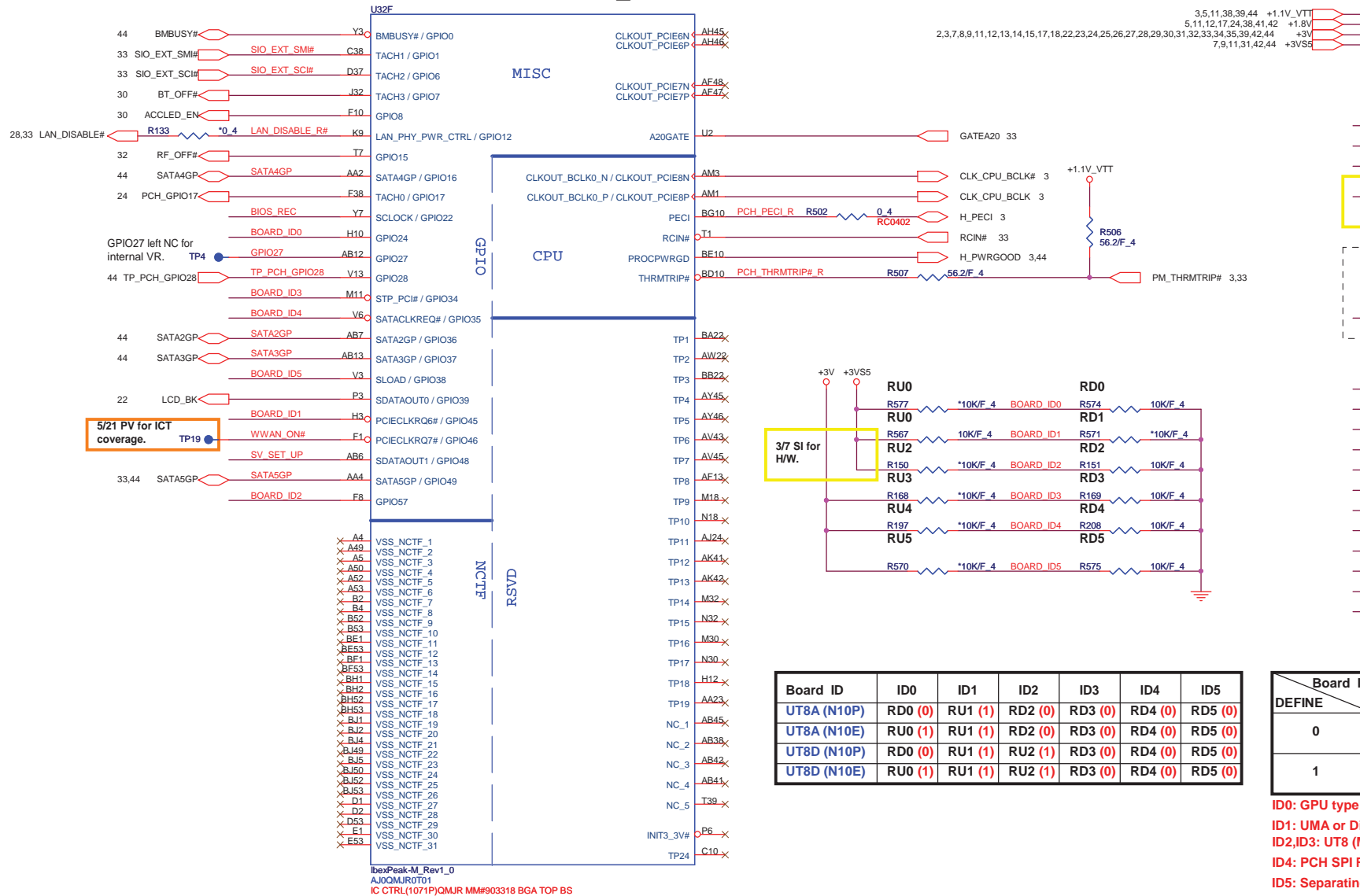












R63 \*10K/F 4 GNT3# 9

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = A16 swap override/Top-Block Swap Override enabled  
High = Default

SV\_SET\_UP R160 10K/F 4 +3V

SV\_SET\_UP 1-X High = Strong (Default)

R96 \*100K/F 4 PCH\_GPIO33 8

2/6 SI remove for Intel recommend.

Flash Descriptor Security Override

BT\_COMBO\_EN# Low = Enabled  
High = Disabled

R75 \*1K/F 4 GNT0# 9  
R83 \*1K/F 4 GNT1# 9

2/6 SI for change to SPI ROM.

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI (Default)

9,12 NV\_ALE R530 \*1K/F 4 +1.8V  
9,12 NV\_CLE R141 \*1K/F 4

Danbury Technology Enabled

NV\_ALE High = Enable  
Low = Disable

DMI Termination Voltage

NV\_CLE Set to Vcc when LOW  
Set to Vcc/2 when HIGH

No Reboot Strap

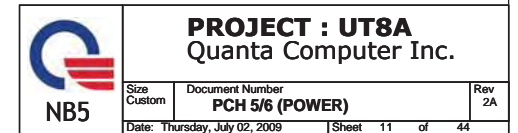
+3V R143 \*1K/F 4 SPKR 8,25

**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom Document Number  
PCH 4/6 (GPIO & Strap)

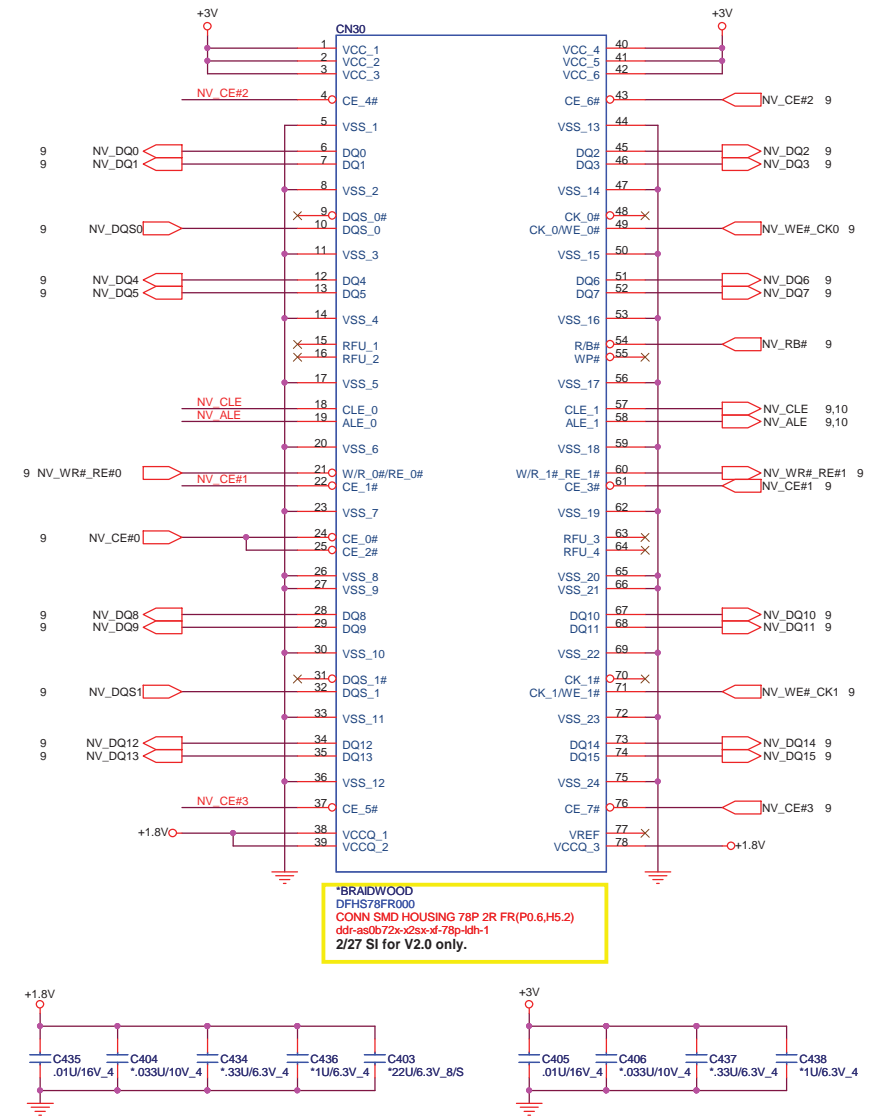
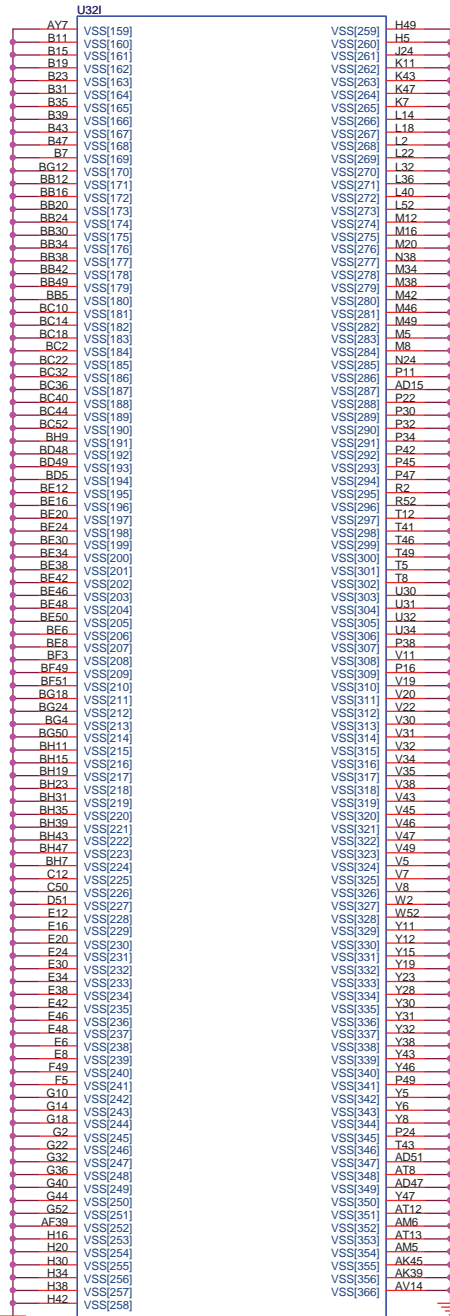
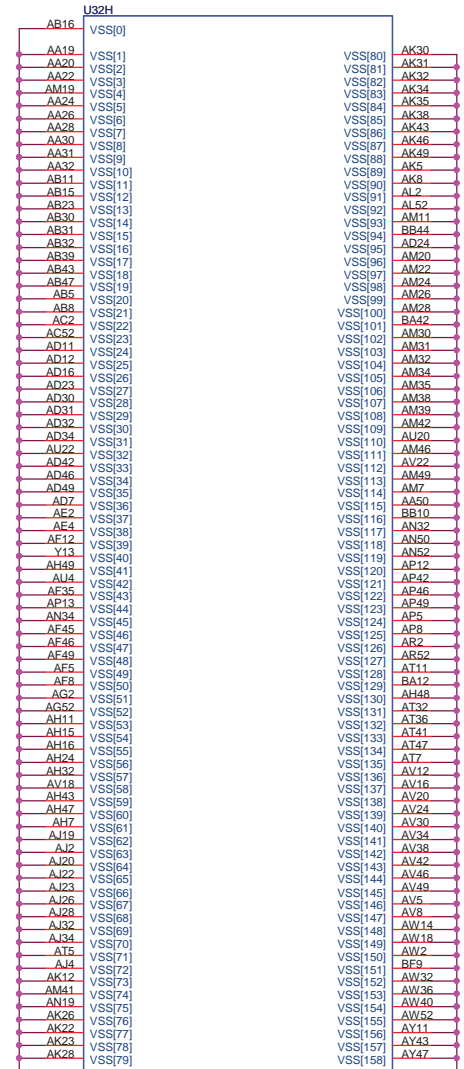
Date: Monday, July 06, 2009 Sheet 10 of 44







IBEX PEAK-M (GND)



\*BRAIDWOOD  
DFHS78FR000  
CONN SMD HOUSING 78P 2R FR(P0.6,H5.2)  
ddr-as0b72x-x2sx-x1-78p-ldh-1  
2/27 SI for V2.0 only.

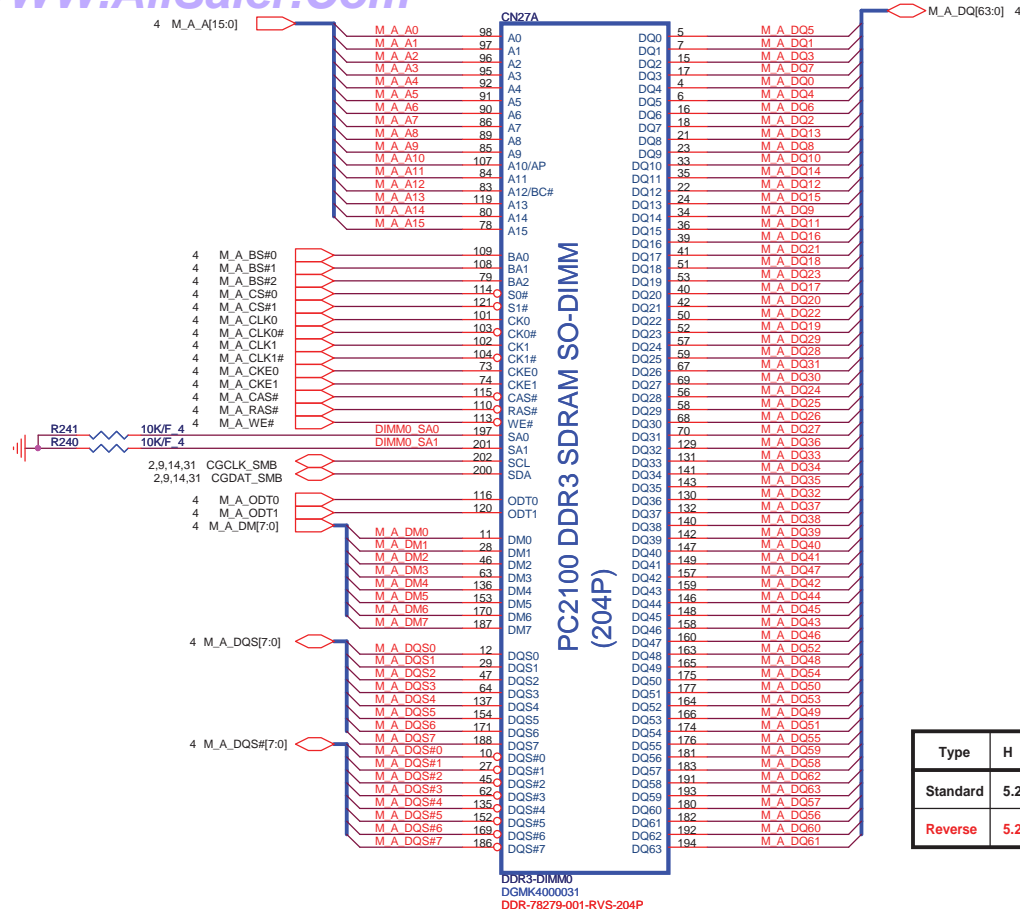
ibexPeak-M\_Rev1\_0  
AJQJMR0T01  
IC CTRL(1071P)QMJR MM#903318 BGA TOP BS

ibexPeak-M\_Rev1\_0  
AJQJMR0T01  
IC CTRL(1071P)QMJR MM#903318 BGA TOP BS

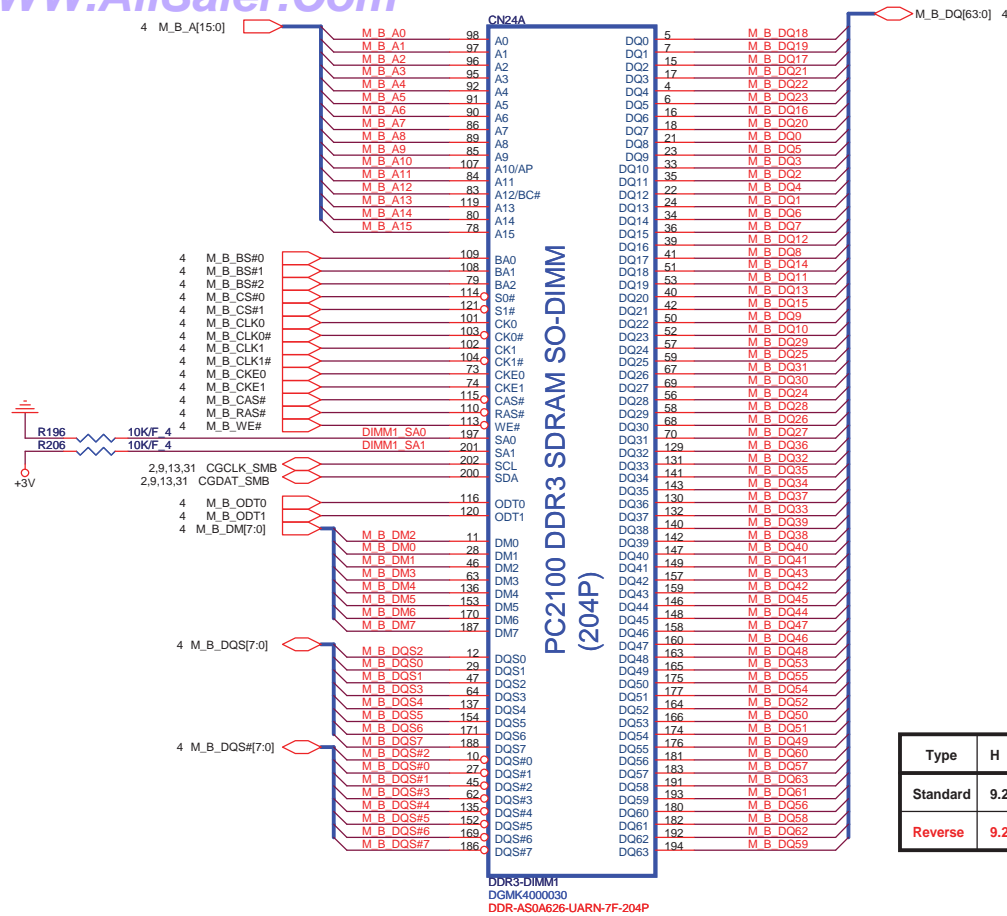
**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>PCH 6/6 (GND) Braidwood</b>	Rev 2A
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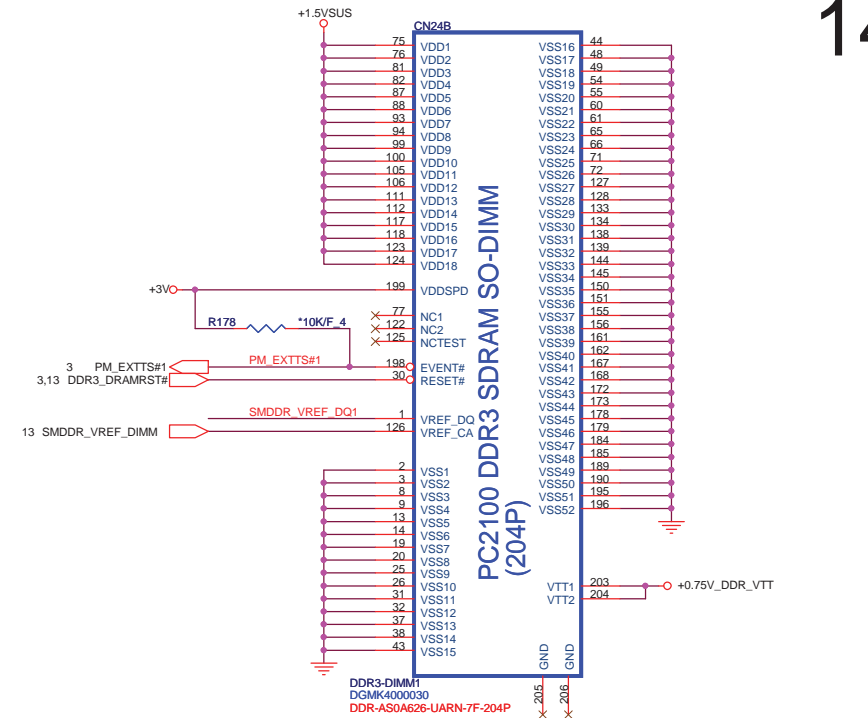




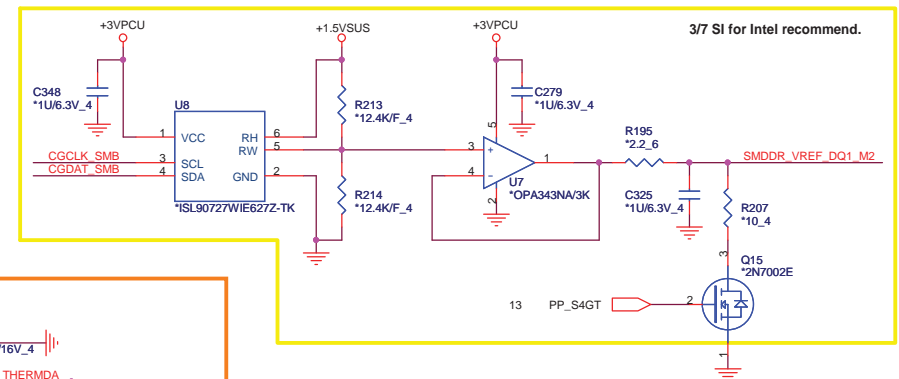
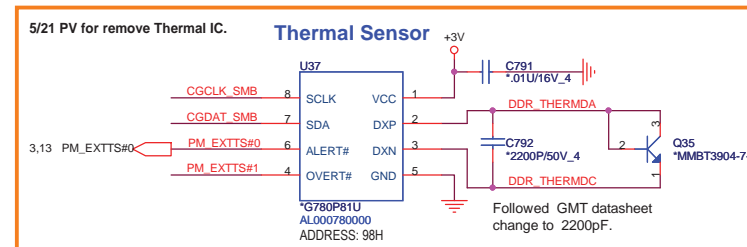
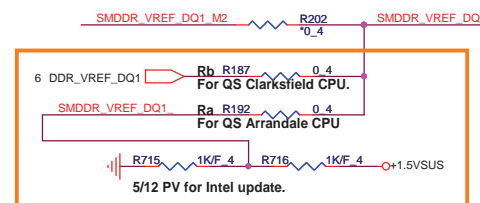
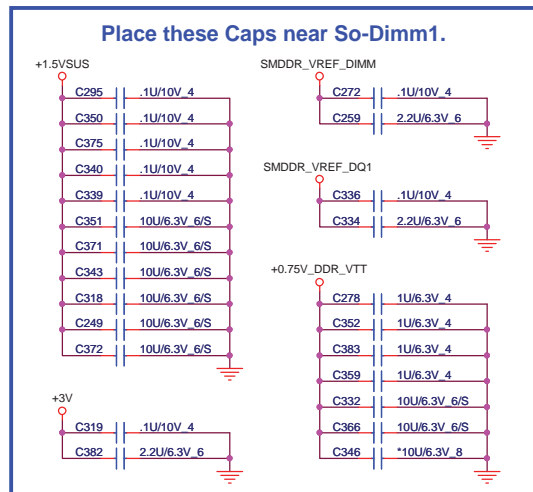
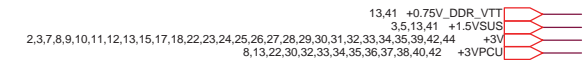




Type	H	Vender	Part Number	Footprint
Standard	9.2	Molex	DGMMK4000003	ddr-c-2013310-204p-1
Reverse	9.2	Foxconn	DGMMK4000030	DDR-AS0A626-UARN-7F-204P



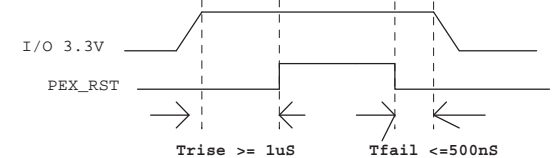
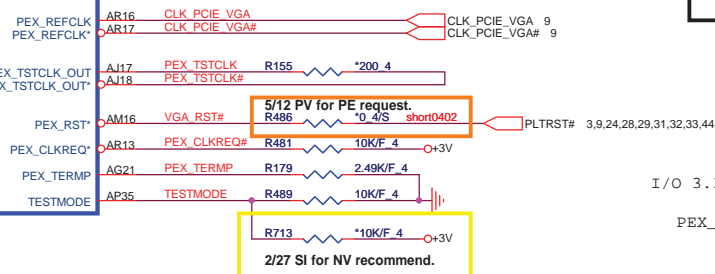
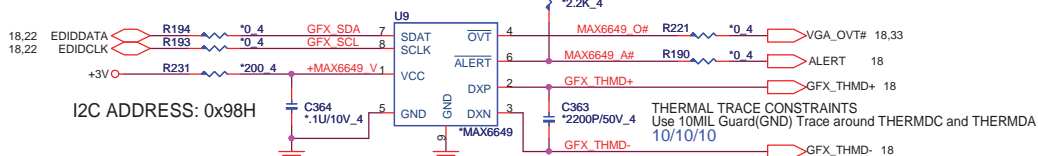
2/23 SI floating for EMI solution.



**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>DDR3 DIMM-1</b>	Rev 2A
Date: Thursday, July 02, 2009   Sheet 14 of 44		

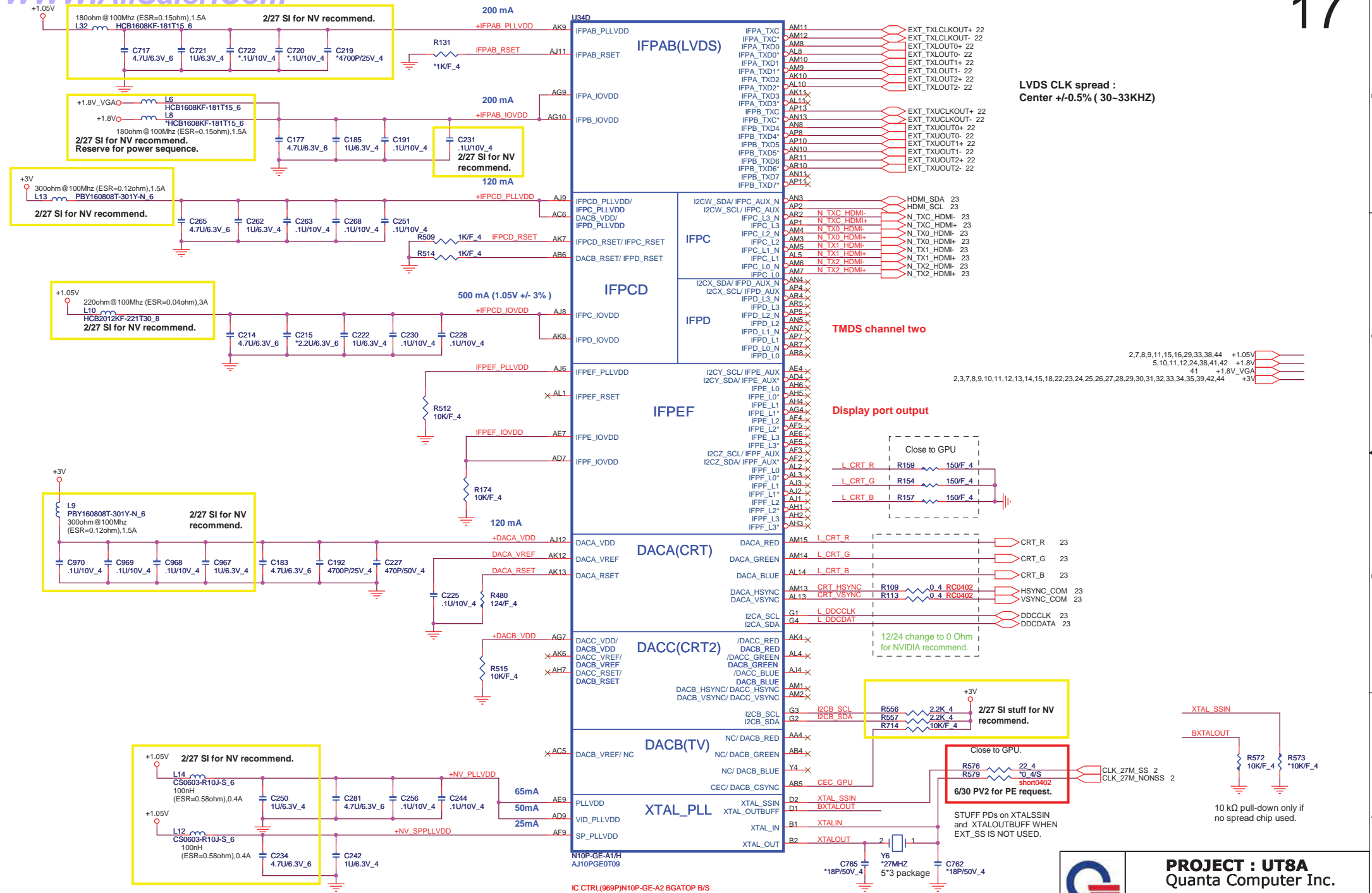




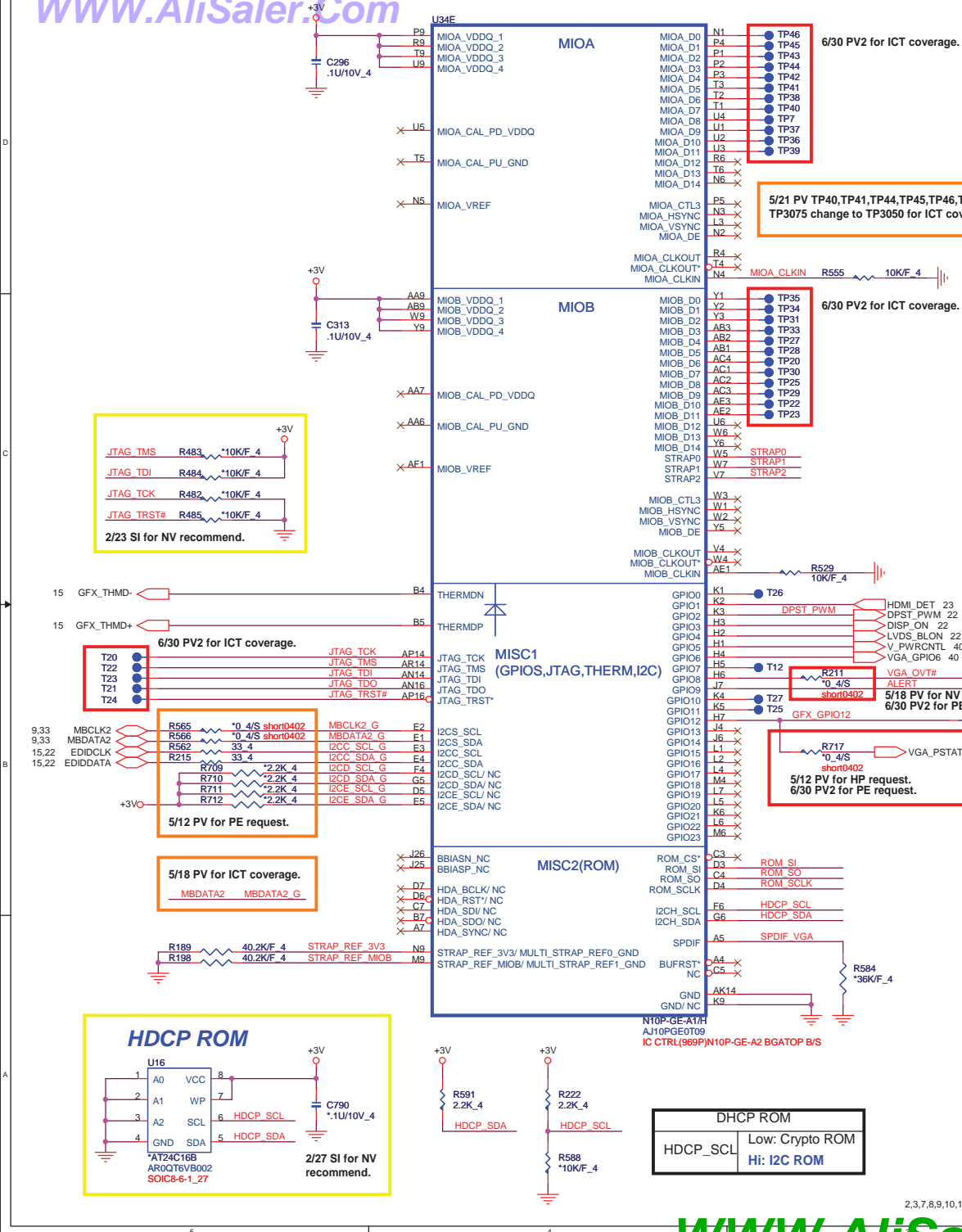










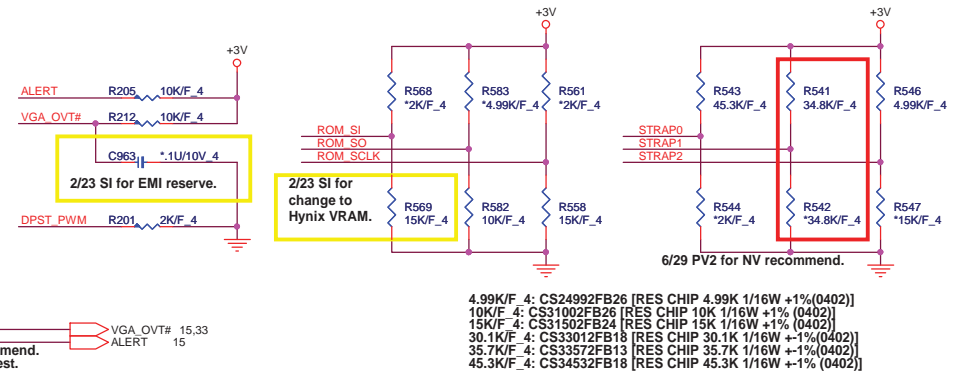


## ***GPIO ASSIGNMENTS***

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

## Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



N10X	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	Default Setting
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DRIVE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

### VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_Si
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix	K4T1G16G3BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung	K4W1G164AE-HC12	PD 20K
0101	GGDDR5 64Mx16x8, 128bit, 1GB, 4Gbps	Qimonda	IDGV1G-05A1F1C-40X	PD 30K
0110	GGDDR5 64Mx16x8, 128bit, 1GB, 4Gbps	Hynix	H5GQ1H24M4FR-TC	PD 35K
0111	GGDDR5 64Mx16x8, 128bit, 1GB, 4Gbps	Samsung	K4G1032ZF5E-HC05	PD 40K
xxxx	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Hynix	H5TQ1G64G3AFR-14C	
xxxx	DDR3 64Mx16x8, 128bit, 1GB, 667MHz	Samsung	K4W1G164AD-EC12	

### PCI\_DEVID[4] & PCI\_DEVID[3:0] Configuration Table

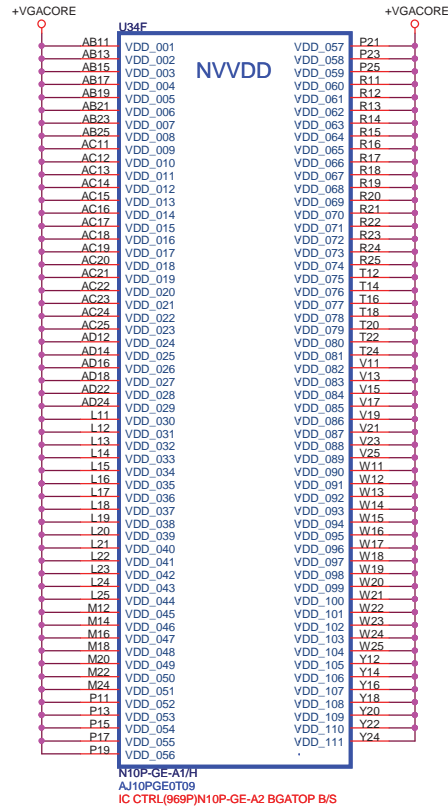
GPU CHIP	PCI_DEVID	ROM_SCLK	STRAP2
N10P-GE	0x0A <b>2 8</b>	<b>0 010 (PD15K)</b>	<b>1000 (PU 5K)</b>
N10E-GE	0x0C <b>A 8</b>	<b>0 010 (PD15K)</b>	<b>1000 (PU 5K)</b>



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Quanta Computer Inc.

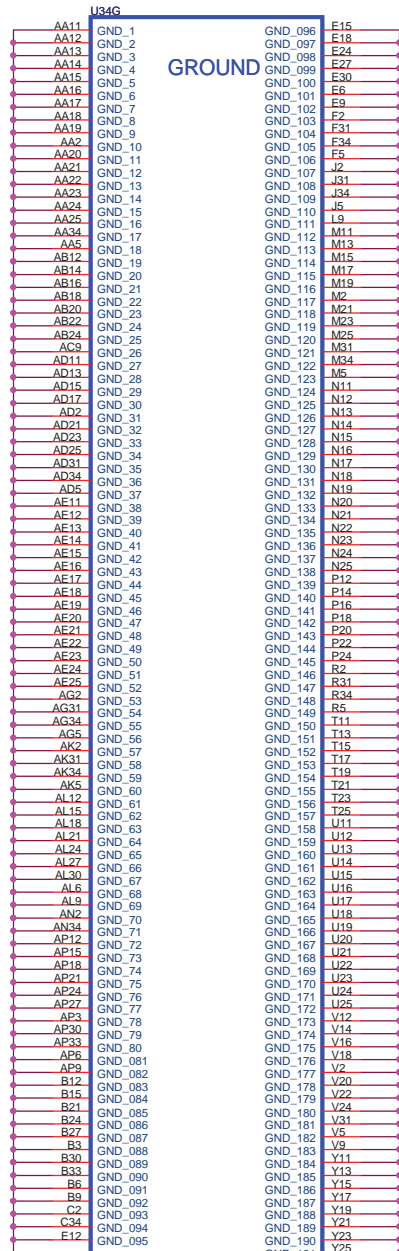
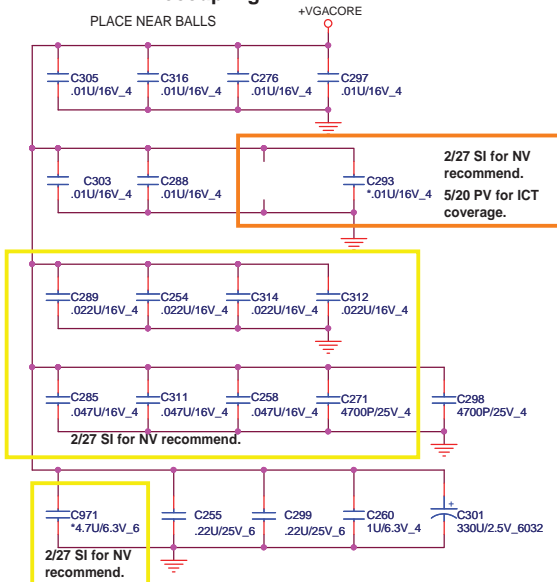
Size Custom	Document Number <b>N10X (GPIO &amp; STRAPS) 4/5</b>	Rev 2A
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### NVVDD Decoupling

PLACE NEAR BALLS

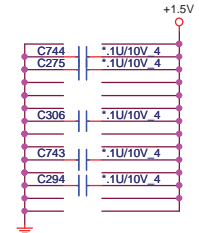


### VRAM A termination

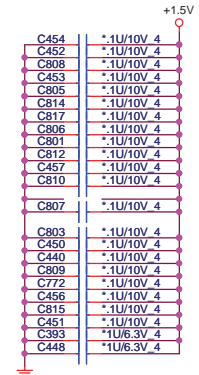
### VRAM C termination

2/6 SI delete All termination for Nvidia recommend.

### VRAM A Bypass CAP



### VRAM C Bypass CAP



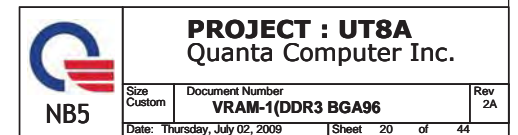
2/27 SI for NV recommend.

40 +VGACORE  
16,20,21,31,32,38,41,42 +1.5V

**PROJECT : UT8A**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>N10X (POWER &amp; GND) 5/5</b>	Rev 2A
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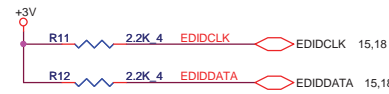
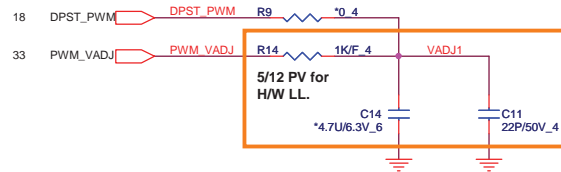
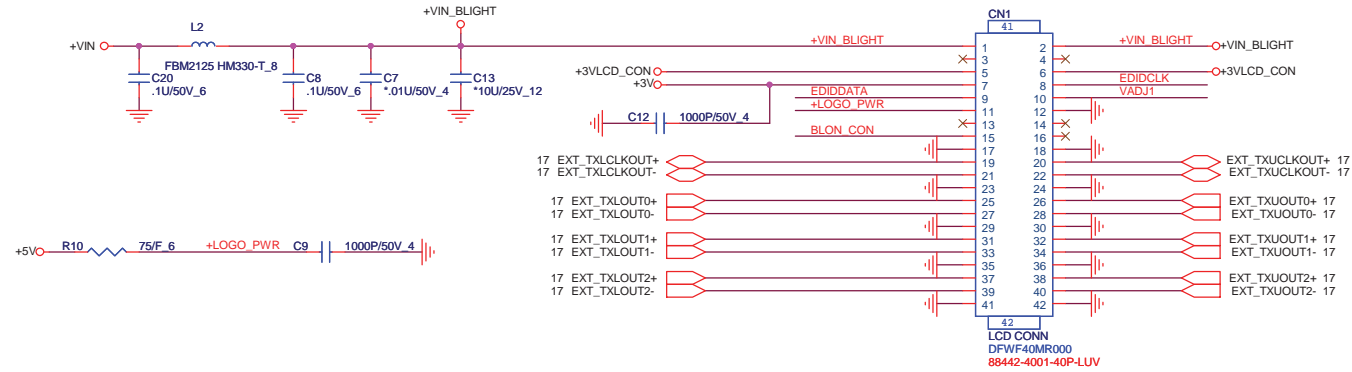




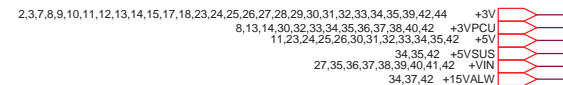
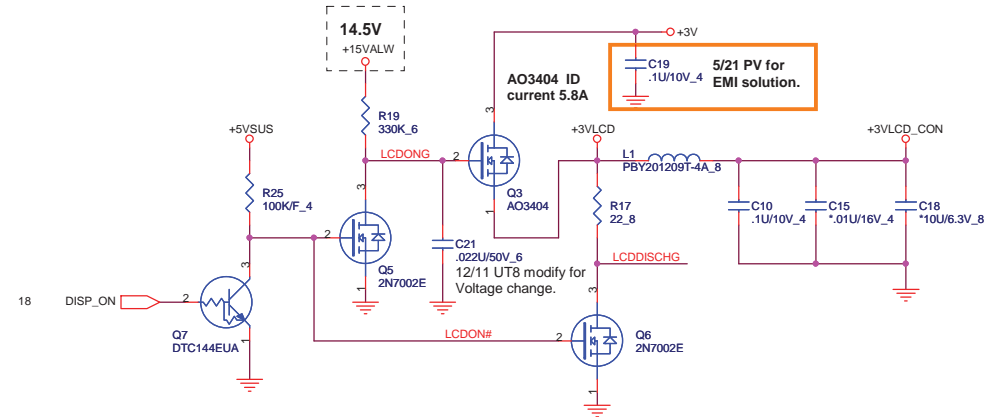
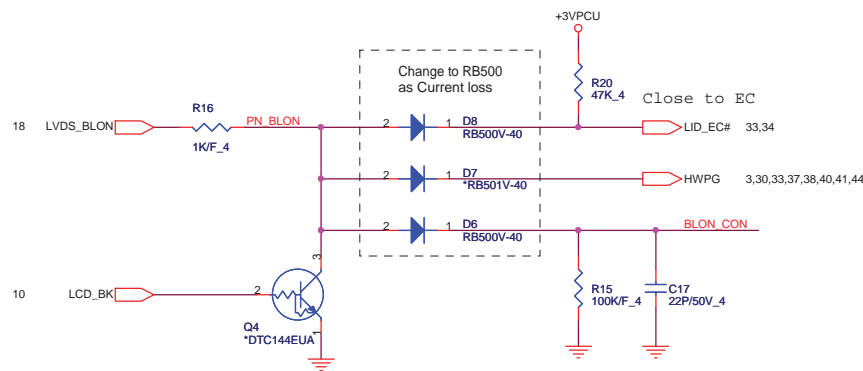






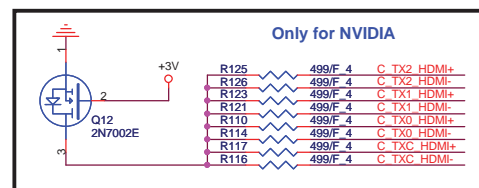
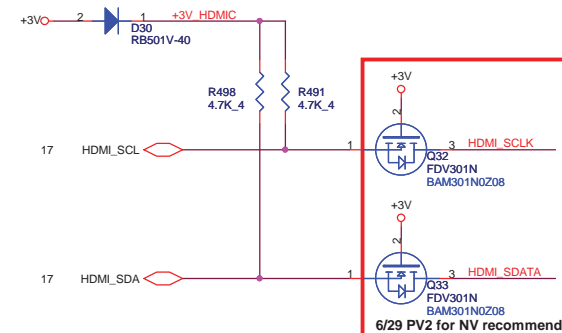
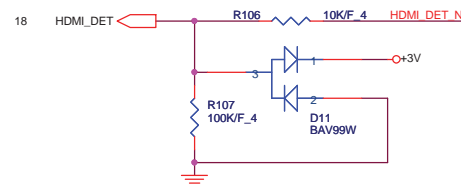
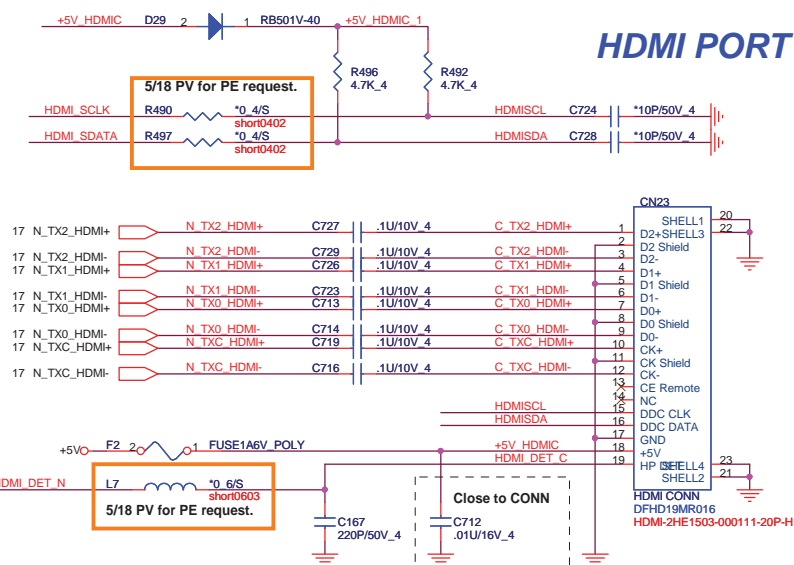
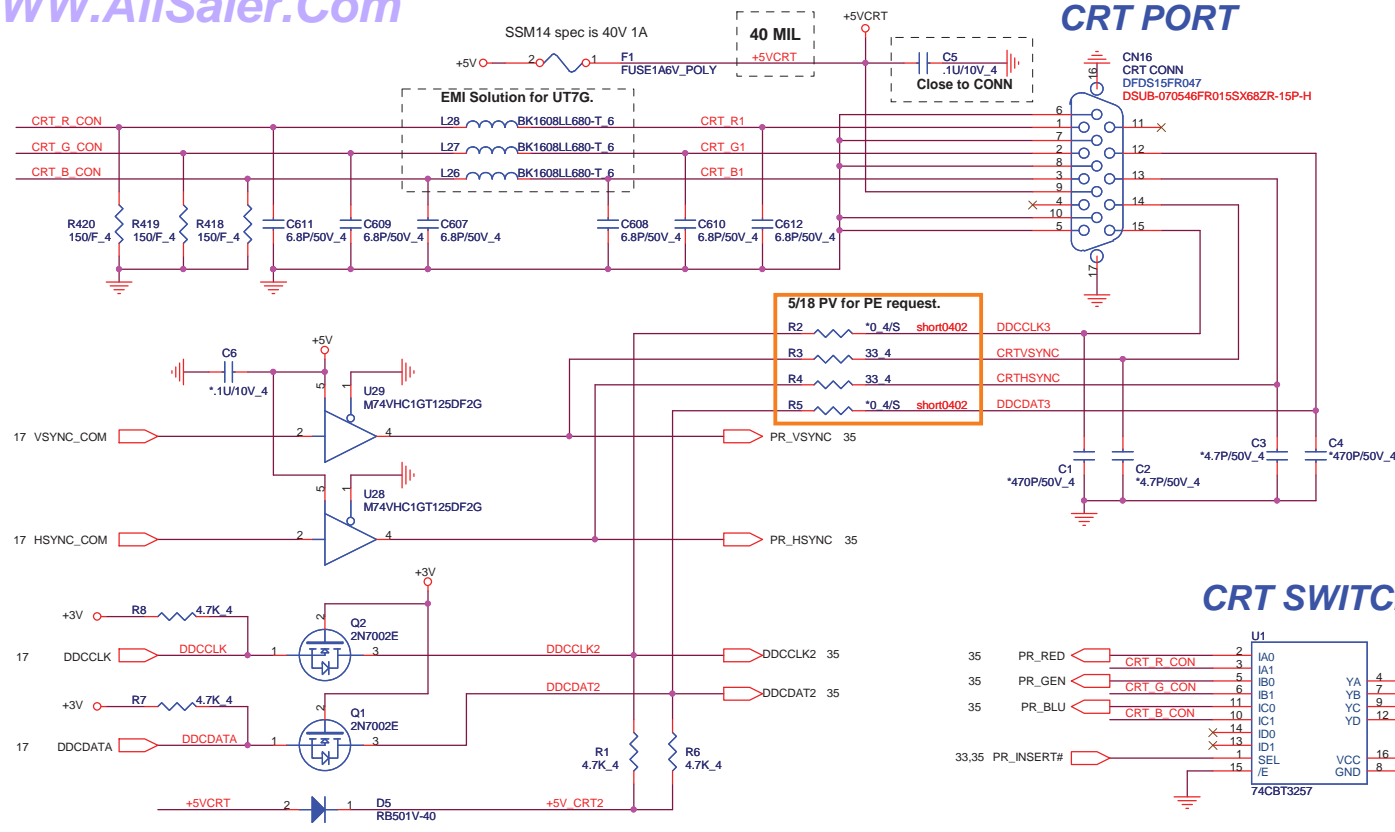


Nvidia suggest:

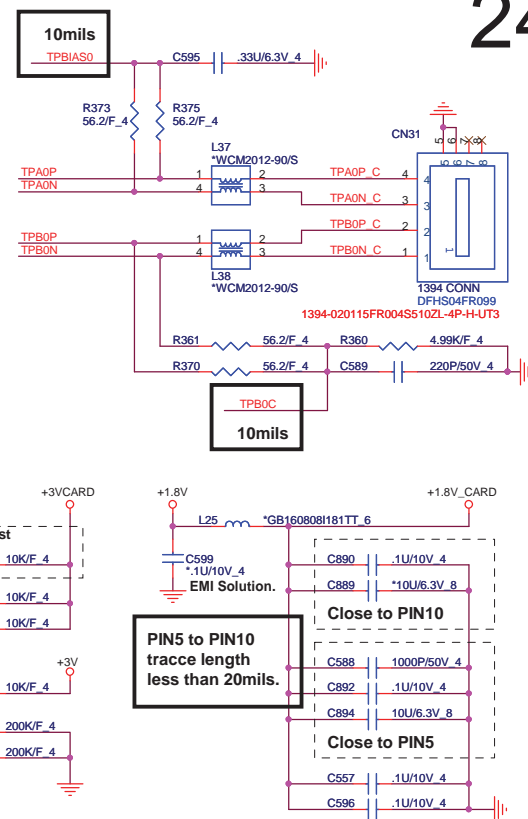
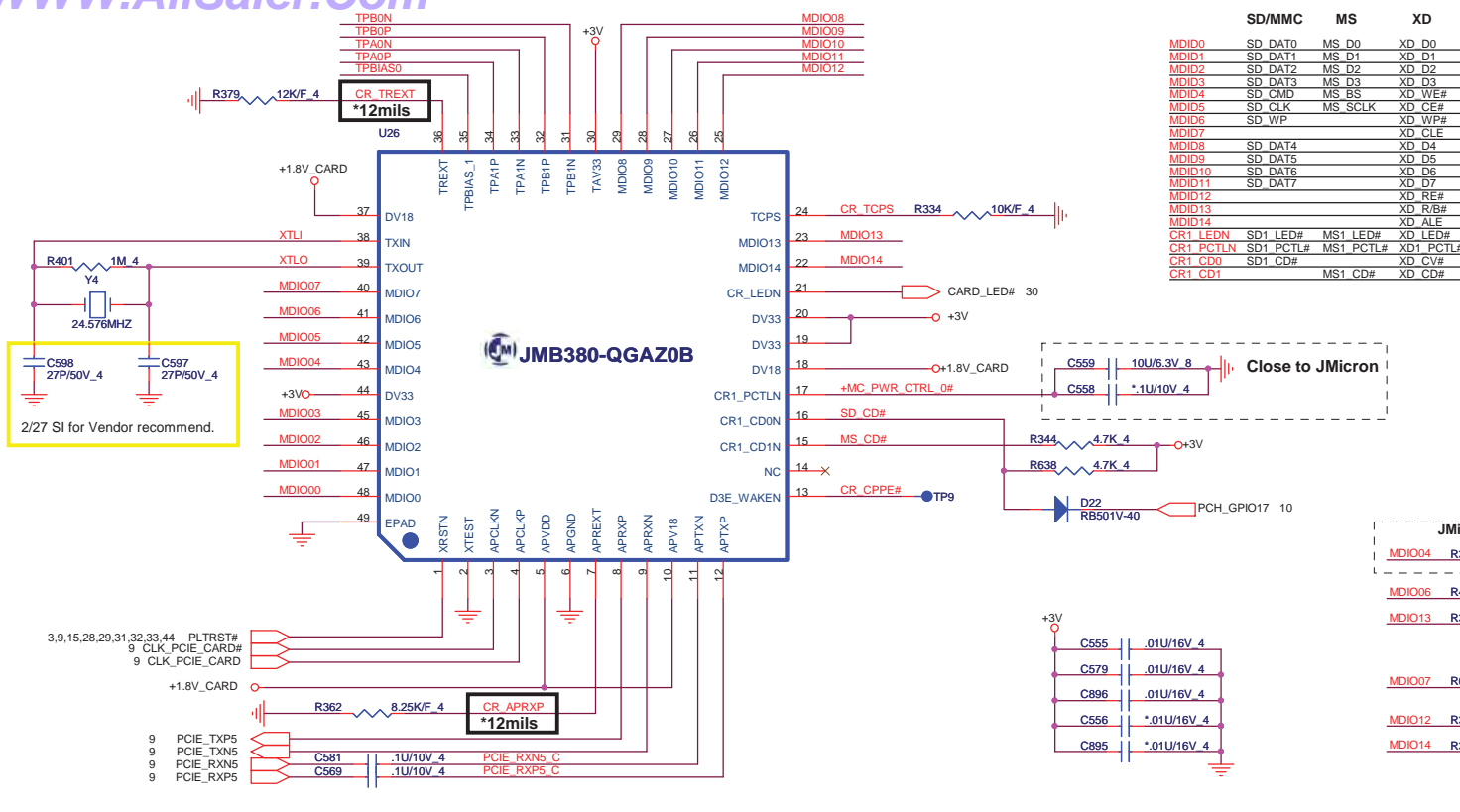


		<b>PROJECT : UT8A</b>	
		Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	LCD CONN/lid function	2A	
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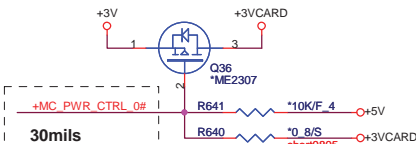
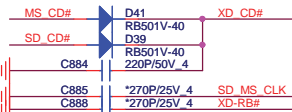
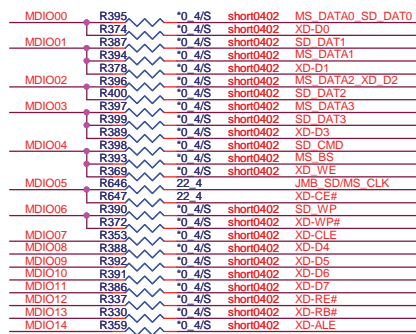
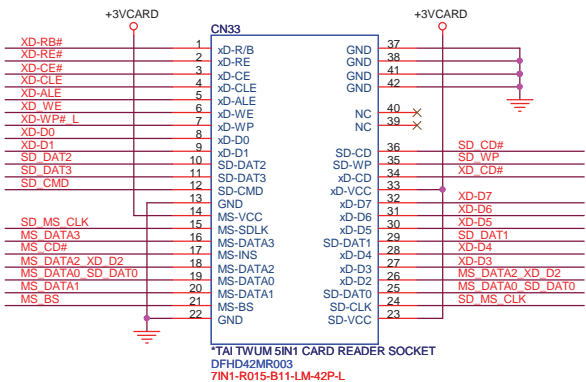
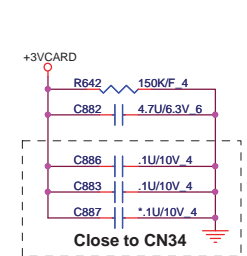
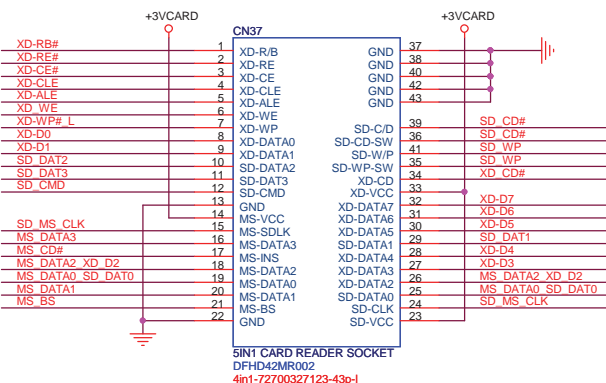








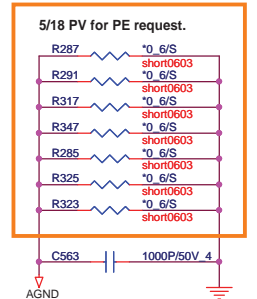
## 5 IN1 CARD READER (XD,MMC/SD,MS/MSP)



**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 2A
	<b>JMB380/CR Socket/1394</b>	
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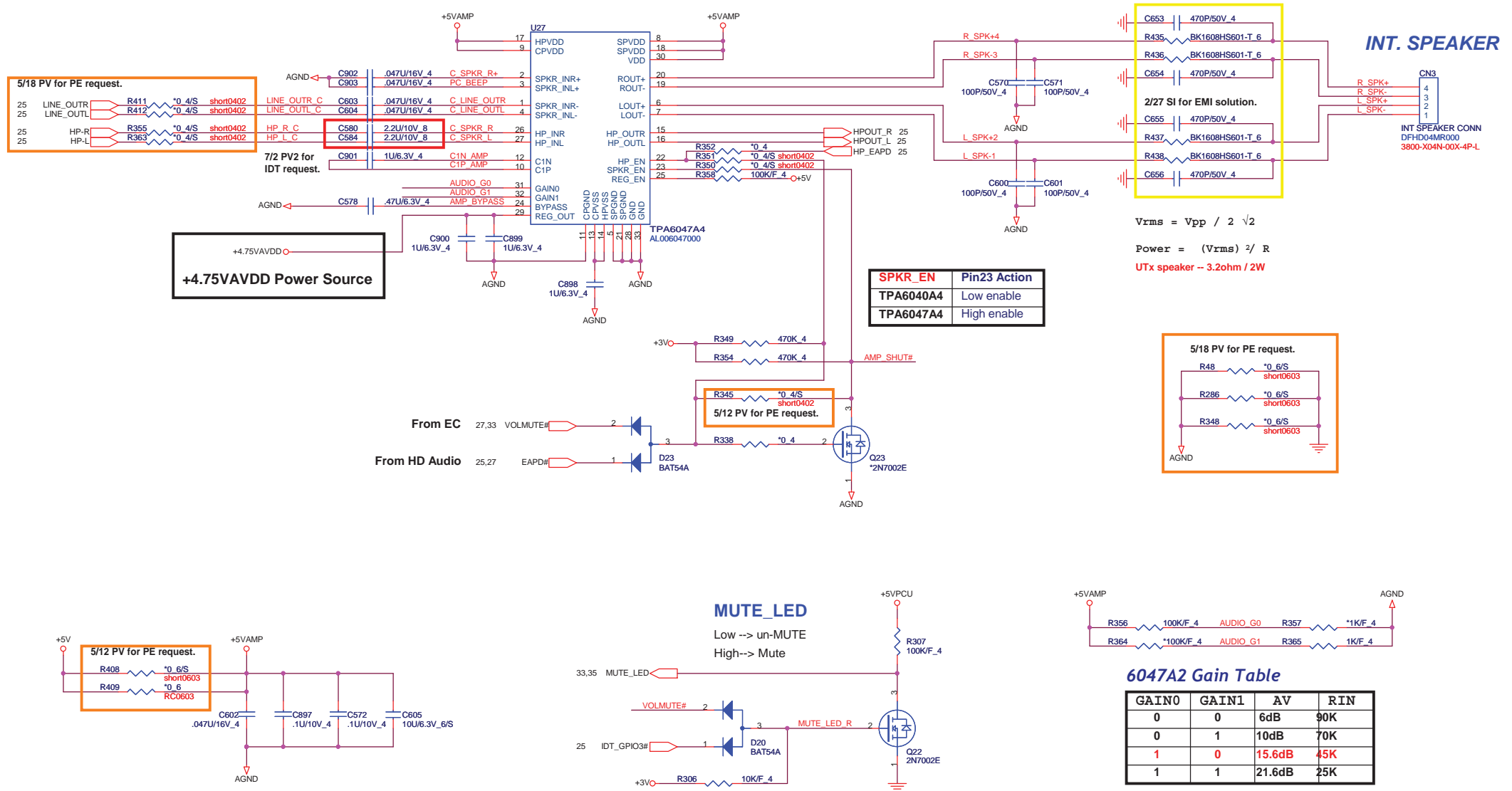




13,26  
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## AUDIO AMPLIFIER



2,3,7,8,9,10,11,12,13,14,15,17,18,22,23,24,25,27,28,29,30,31,32,33,34,35,39,42,44

+3V

25,27 +4.75VAVDD

+5V

13,25,33,37,38,39,40,41,42

+5VPCU

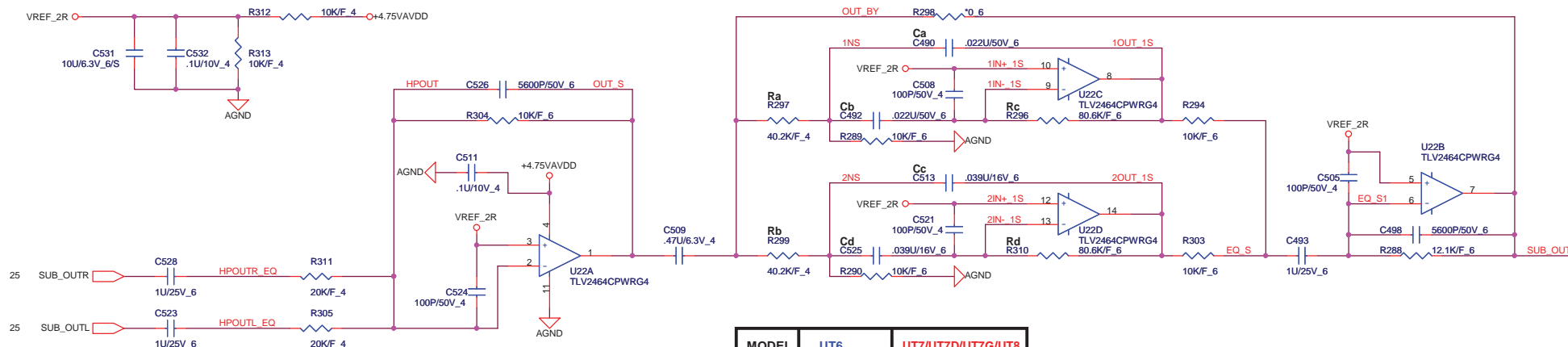
27 +5VAMP



**PROJECT : UT8A**  
Quanta Computer Inc.

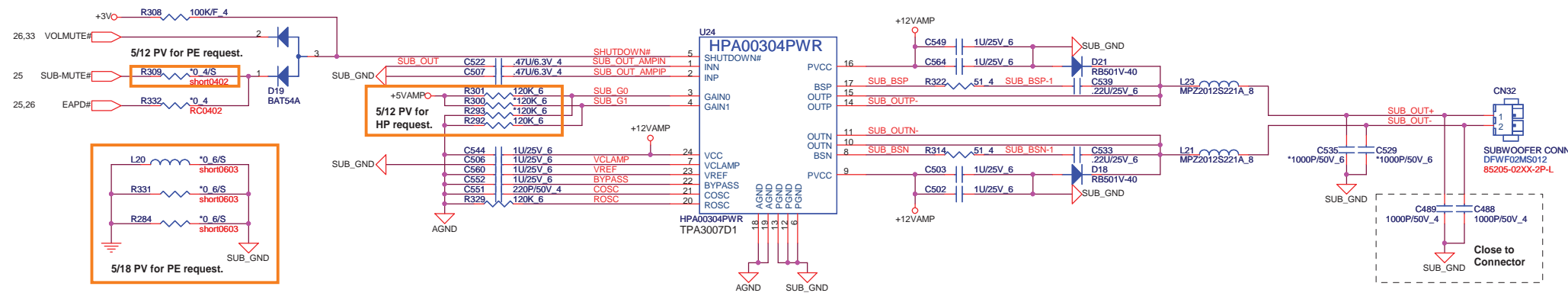
Size Custom Document Number  
**AMP TPA6047/Speaker** Rev 2A  
Date: Thursday, July 02, 2009 Sheet 26 of 44





MODEL	UT6	UT7/UT7D/UT7G/UT8
Ra	60.4K/F_6	40.2K/F_4
Rb	60.4K/F_6	40.2K/F_4
Rc	60.4K/F_6	80.6K/F_6
Rd	60.4K/F_6	80.6K/F_6
Ca	0.027U/25V_6	0.022U/50V_6
Cb	0.027U/25V_6	0.022U/50V_6
Cc	0.027U/25V_6	0.039U/16V_6
Cd	0.027U/25V_6	0.039U/16V_6

## Sub-Woofer power



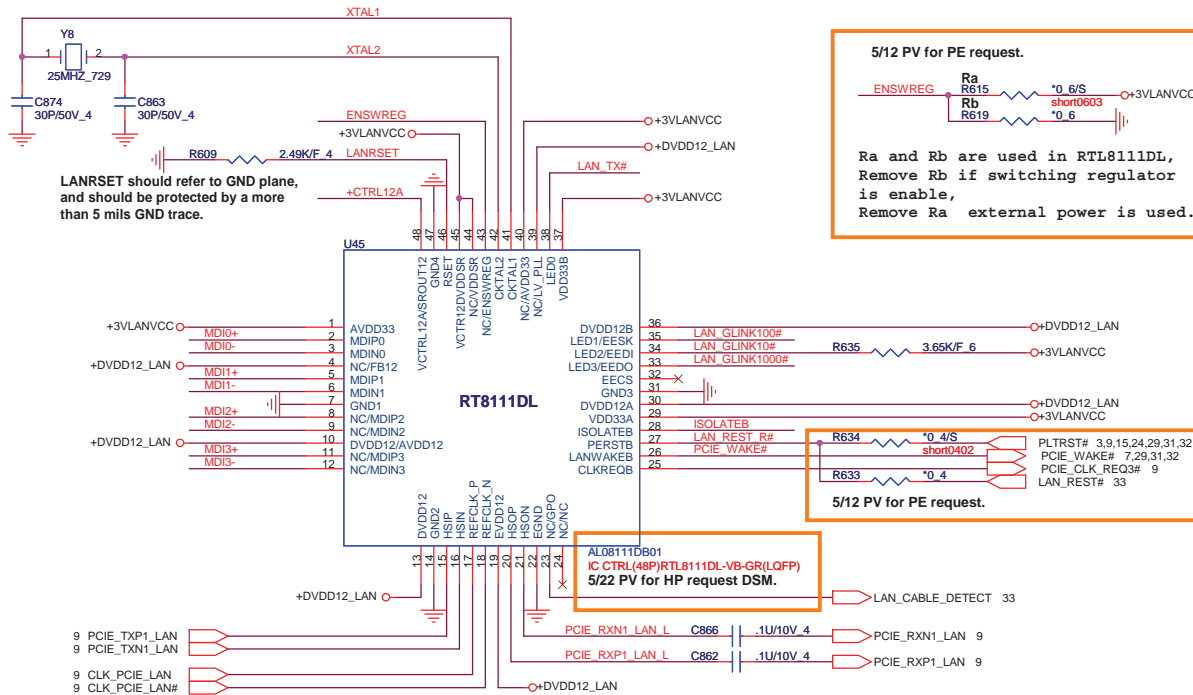
GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

2,3,7,8,9,10,11,12,13,14,15,17,18,22,23,24,25,26,28,29,30,31,32,33,34,35,39,42,44  
25,26 +4.75VAVDD  
26 +5VAMP  
22,35,36,37,38,39,40,41,42 +VIN

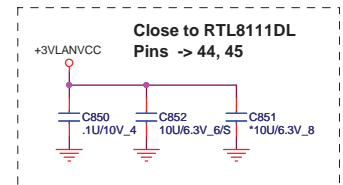
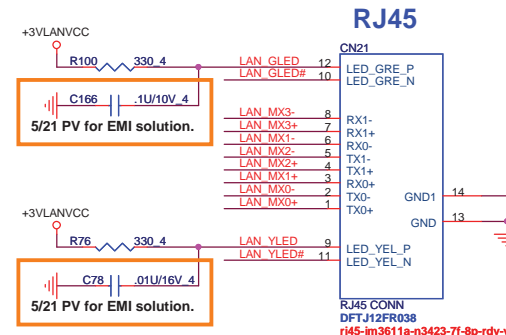
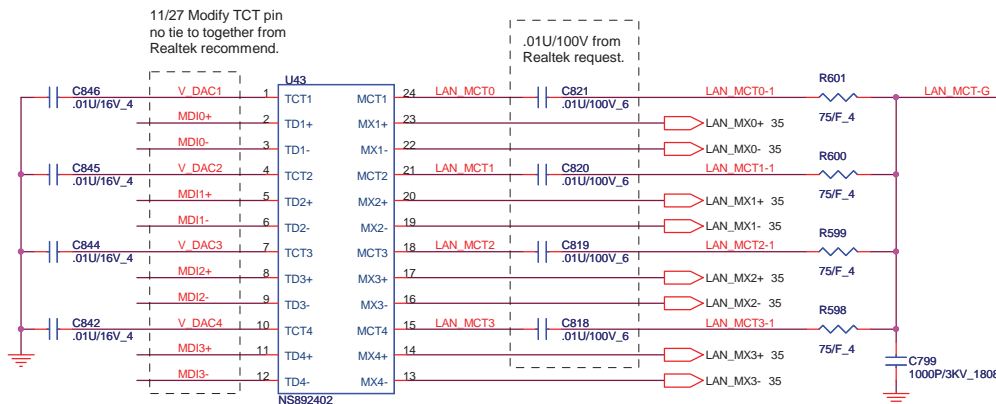
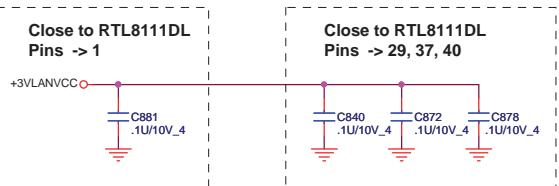
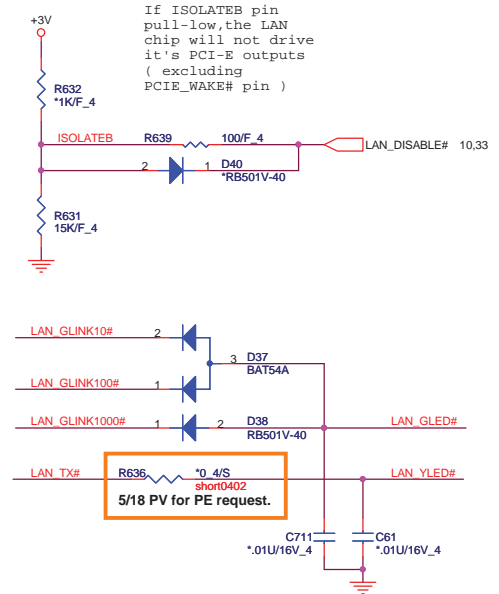
**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 2A
SUBWOOFER(EQ & AMP.)		
Date: Thursday, July 02, 2009	Sheet 27 of 44	

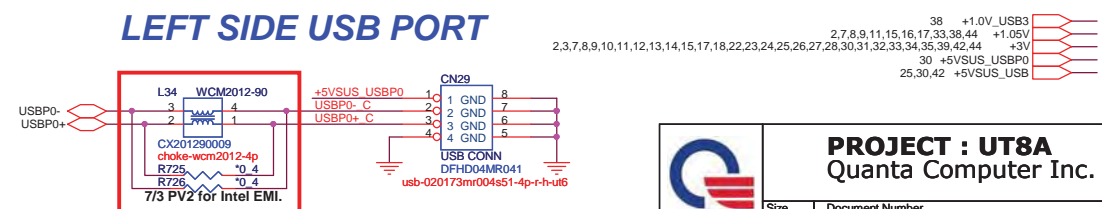
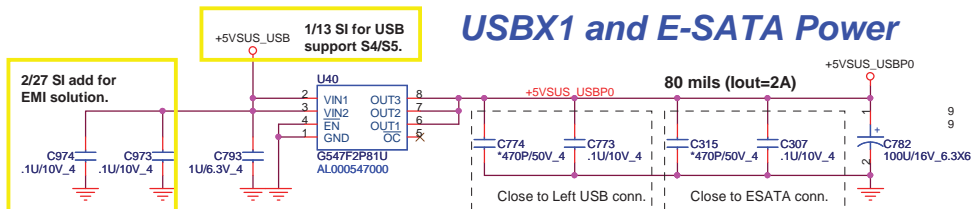
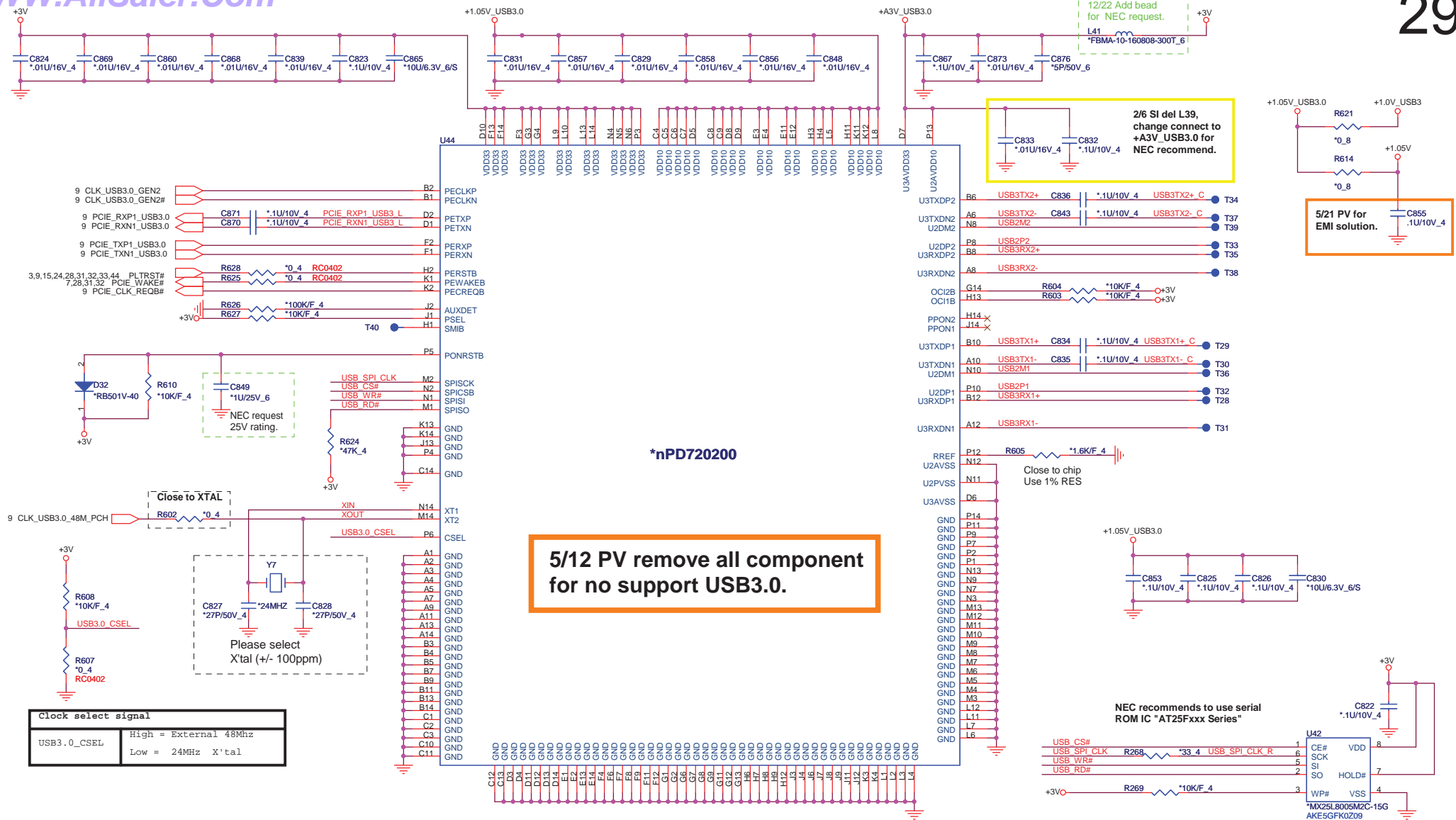




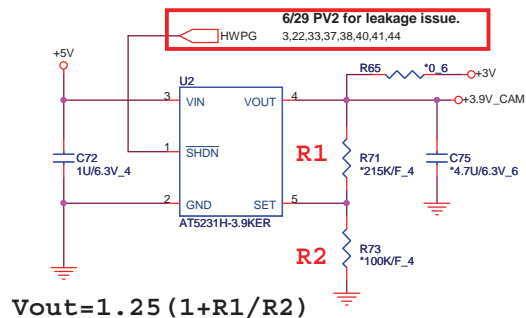
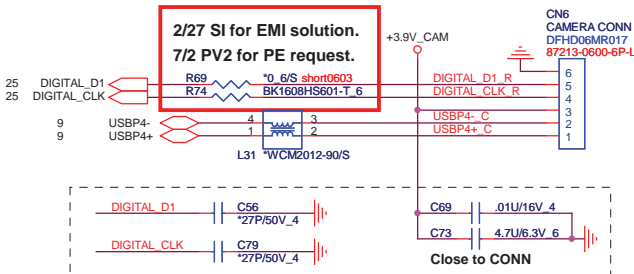
2,3,7,8,9,10,11,12,13,14,15,17,18,22,23,24,25,26,27,29,30,31,32,33,34,35,39,42,44 +3V  
42 +3VLANVCC



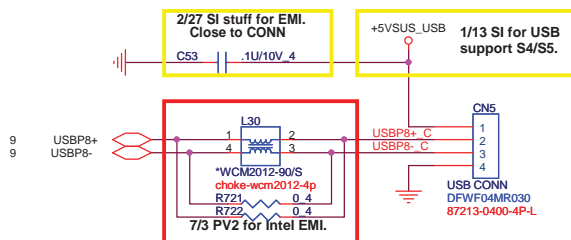




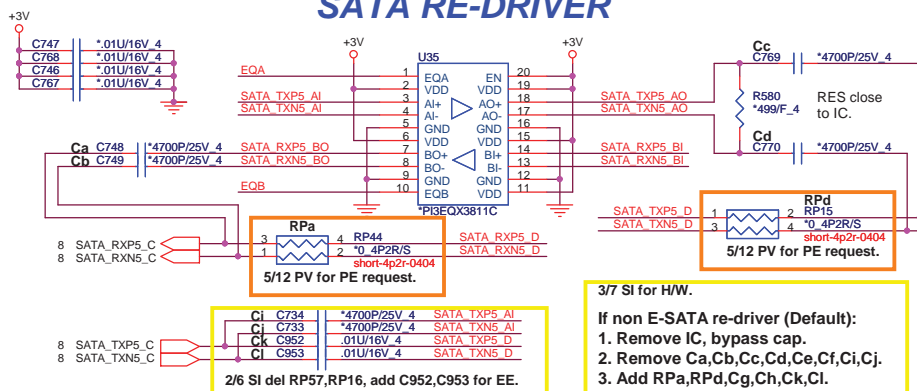




**RIGHT SIDE USB CONN x1**



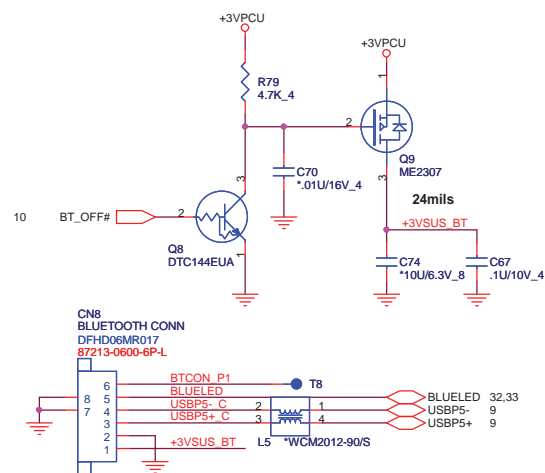
## SATA RE-DRIVER



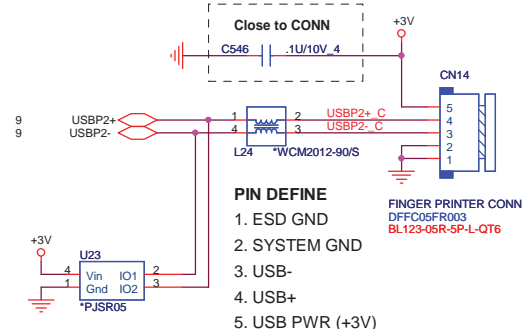
3/7 SI for H/W.

- If non E-SATA re-driver (Default):**
1. Remove IC, bypass cap.
  2. Remove Ca,Cb,Cc,Cd,Ce,Cf,Ci,Cj.
  3. Add RPa,RPd,Cq,Ch,Ck,Cl.

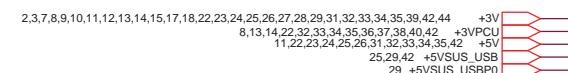
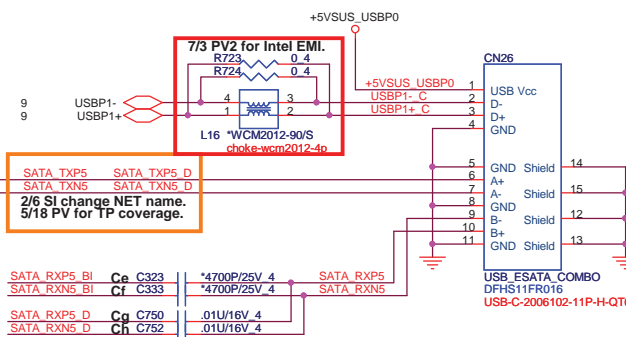
## BLUETOOTH



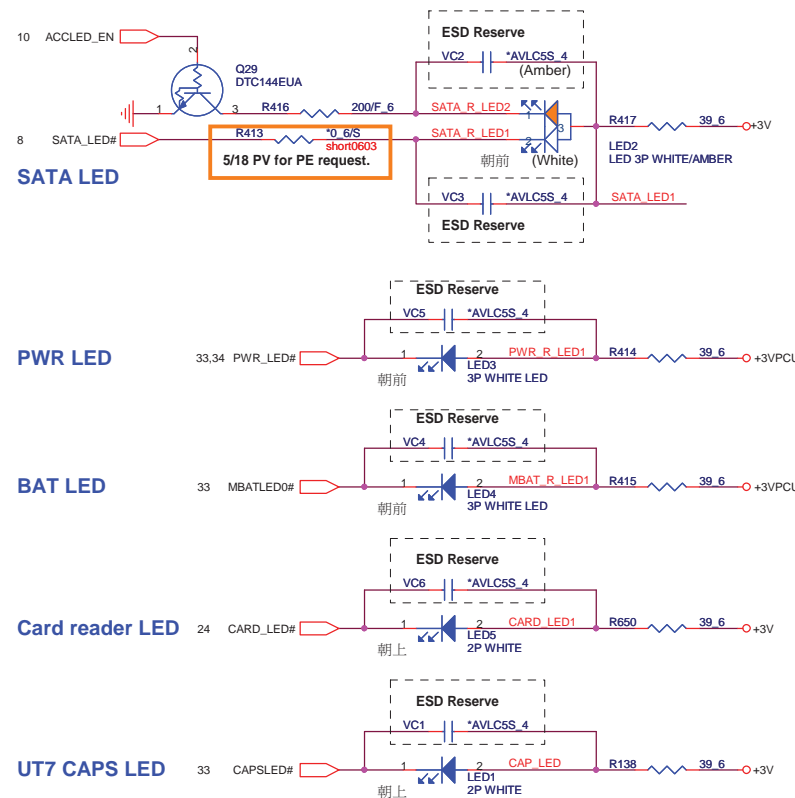
## USB Fingerprint



## LEFT SIDE USB & E-SATA



**LED**



EQx	Compliance Channel
0	3.5dB +/- 1.0dB
1	6.5dB +/- 1.0dB



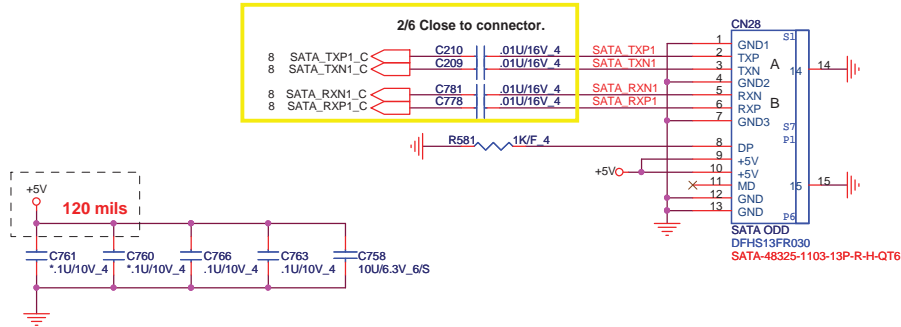
**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>BT/WC/FT/ESATA/USB/LED</b>	Rev 2A
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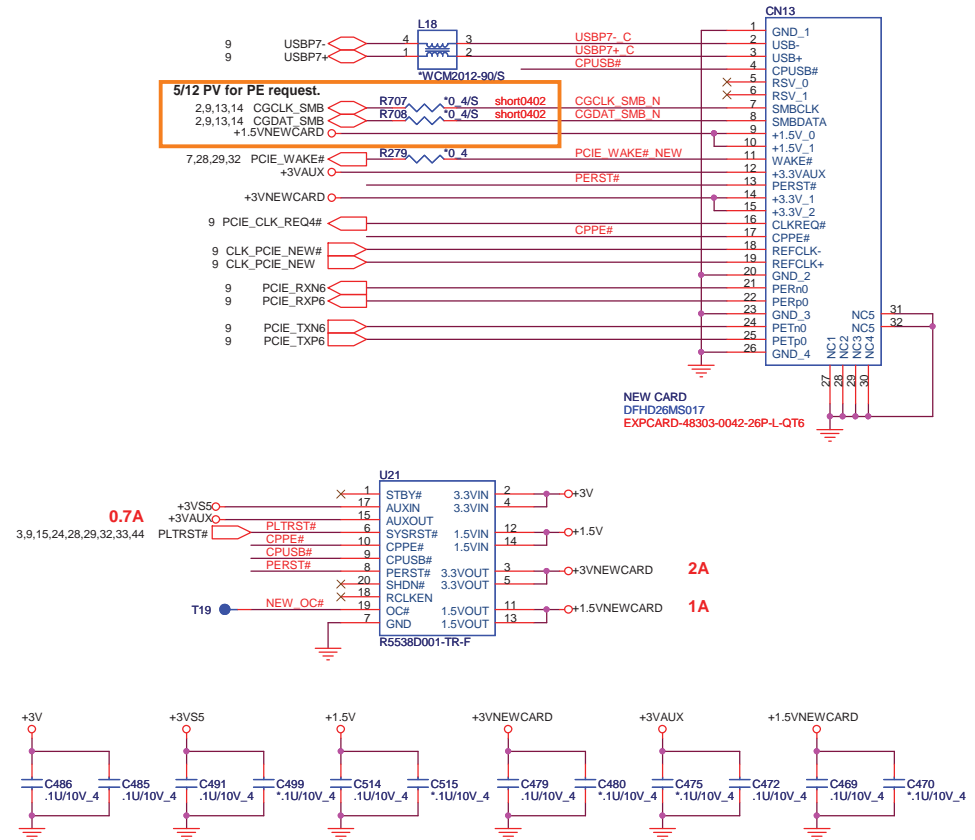
## SATA CD-ROM

16,19,20,21,32,38,41,42 +1.5V  
2,3,7,8,9,10,11,12,13,14,15,17,18,22,23,24,25,26,27,28,29,30,32,33,34,35,39,42,44 +3V  
7,9,10,11,42,44 +3VSS  
11,22,23,24,25,26,30,32,33,34,35,42 +5V

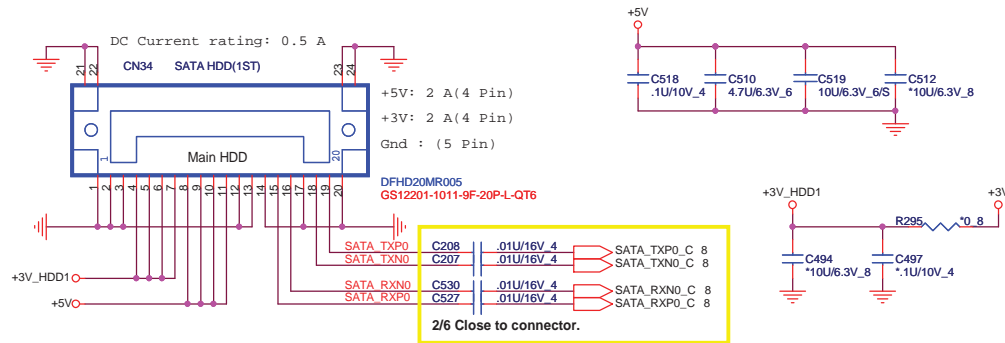


## NEWCARD (PCIEXPRESS\*1 + USB\*1)

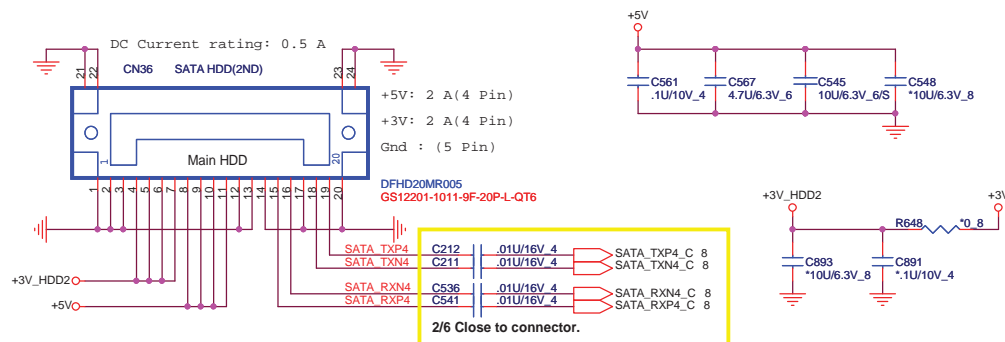
31



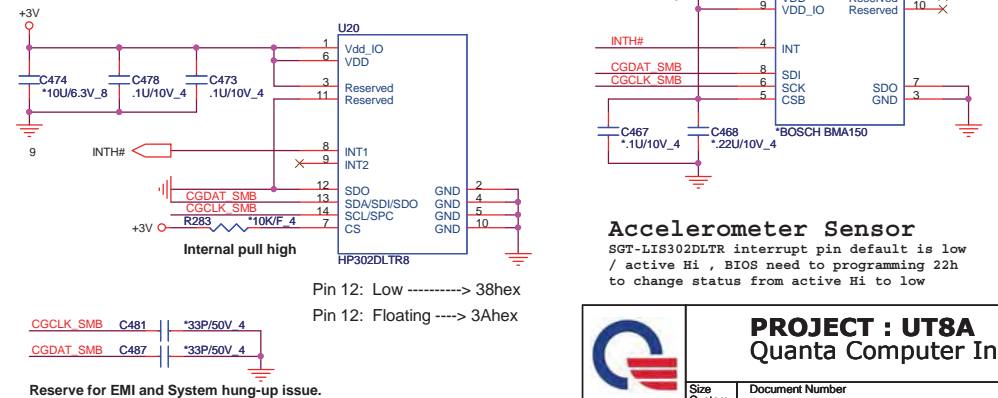
## SATA\_1 CONNECTOR



## SATA\_2 CONNECTOR



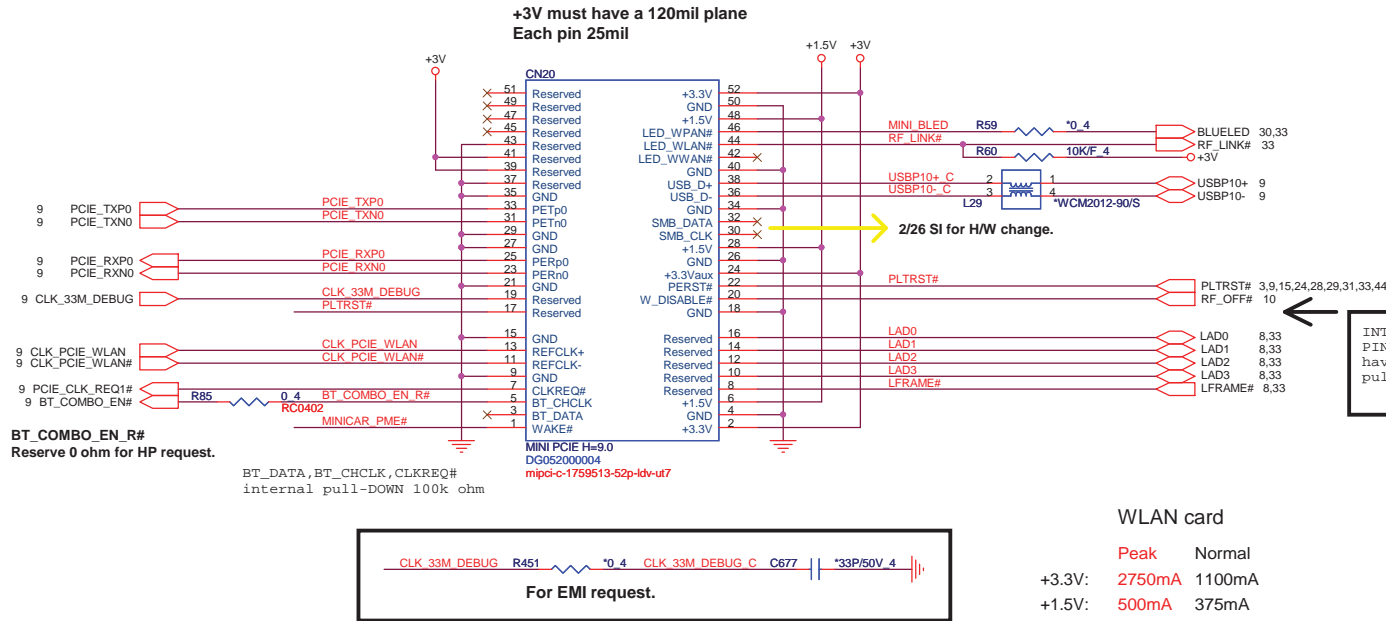
## Accelerometer Sensor



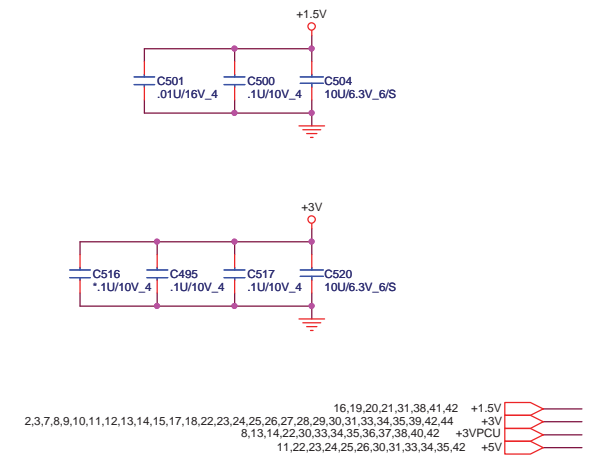
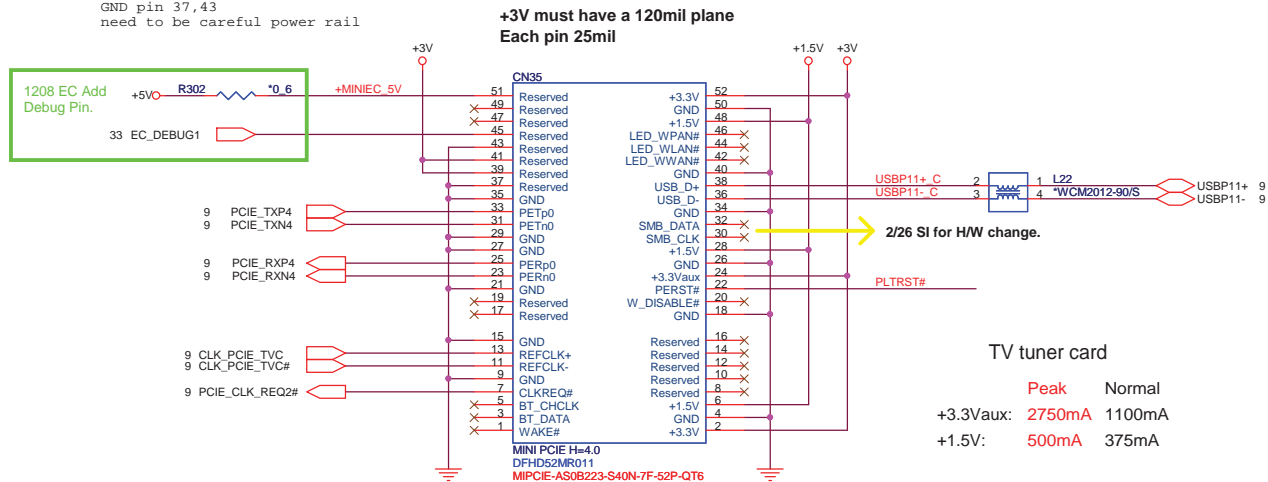
Accelerometer Sensor  
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



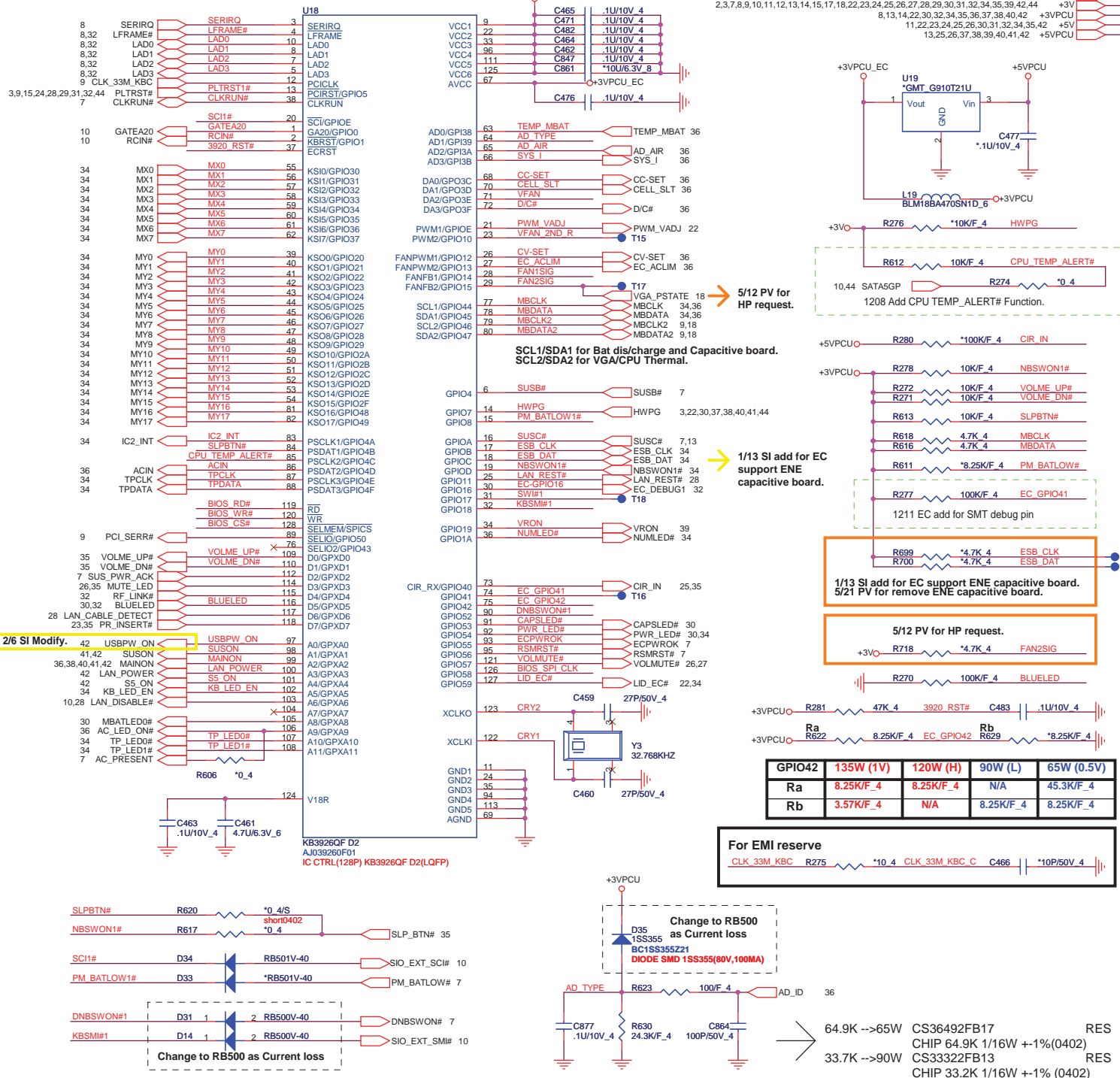
## MINI PCI-E Card 1 (WLAN)



## MINI PCI-E Card 2 (TV Tuner)











## KEYBOARD CONNECTOR



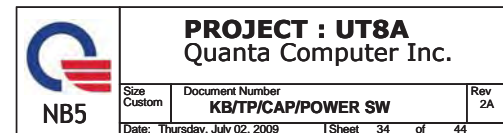
## POWER BOTTON CONNECTOR



## CAP SW CONNECTOR

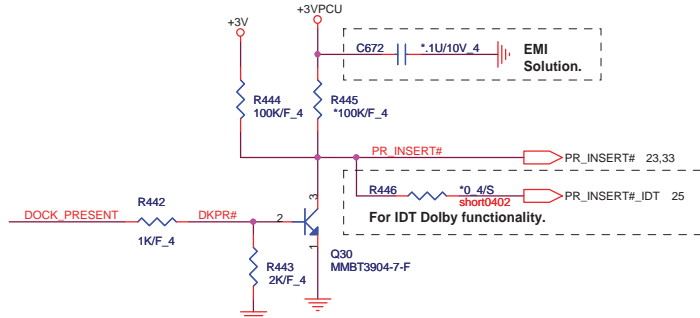
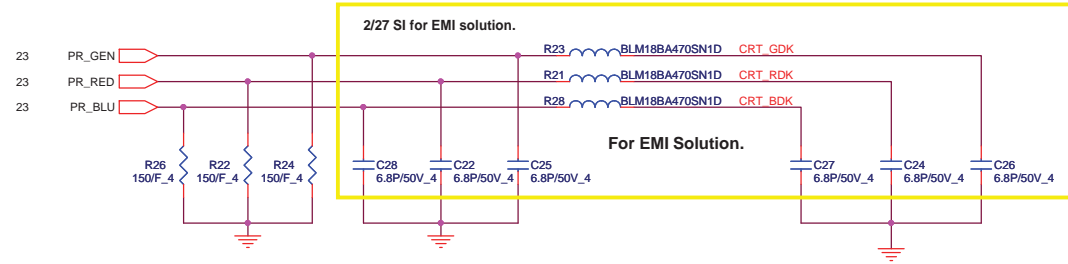
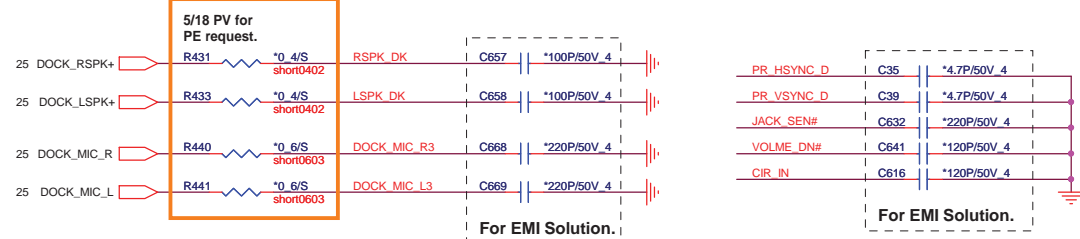
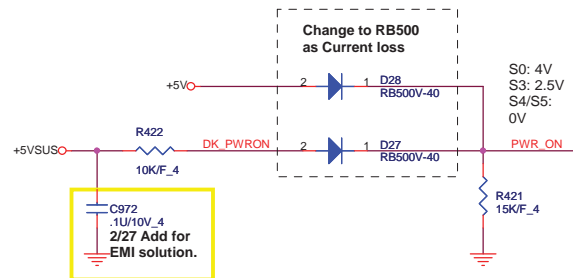
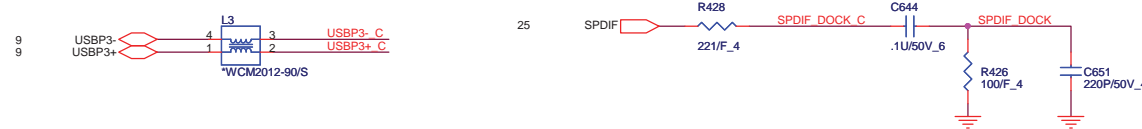
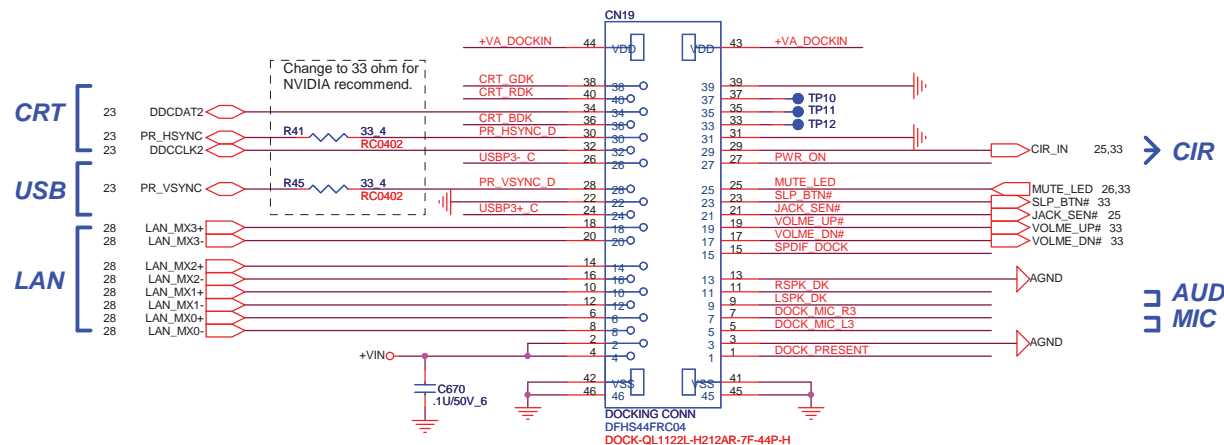
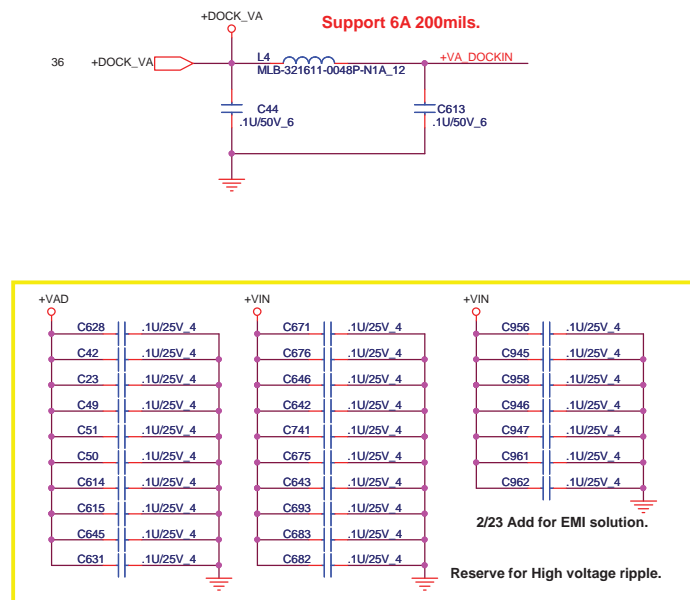


2/27 SI stuff for EMI solution.





# CABLE DOCKING

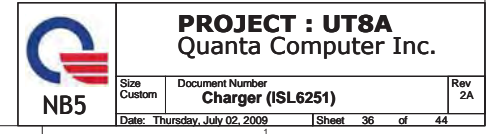


2,3,7,8,9,10,11,12,13,14,15,17,18,22,23,24,25,26,27,28,29,30,31,32,33,34,39,42,44 +3V  
8,13,14,22,30,32,33,34,36,37,38,40,42 +3VPCU  
11,22,23,24,25,26,30,31,32,33,34,42 +5V  
22,34,42 +5VSUS  
22,27,36,37,38,39,40,41,42 +VIN

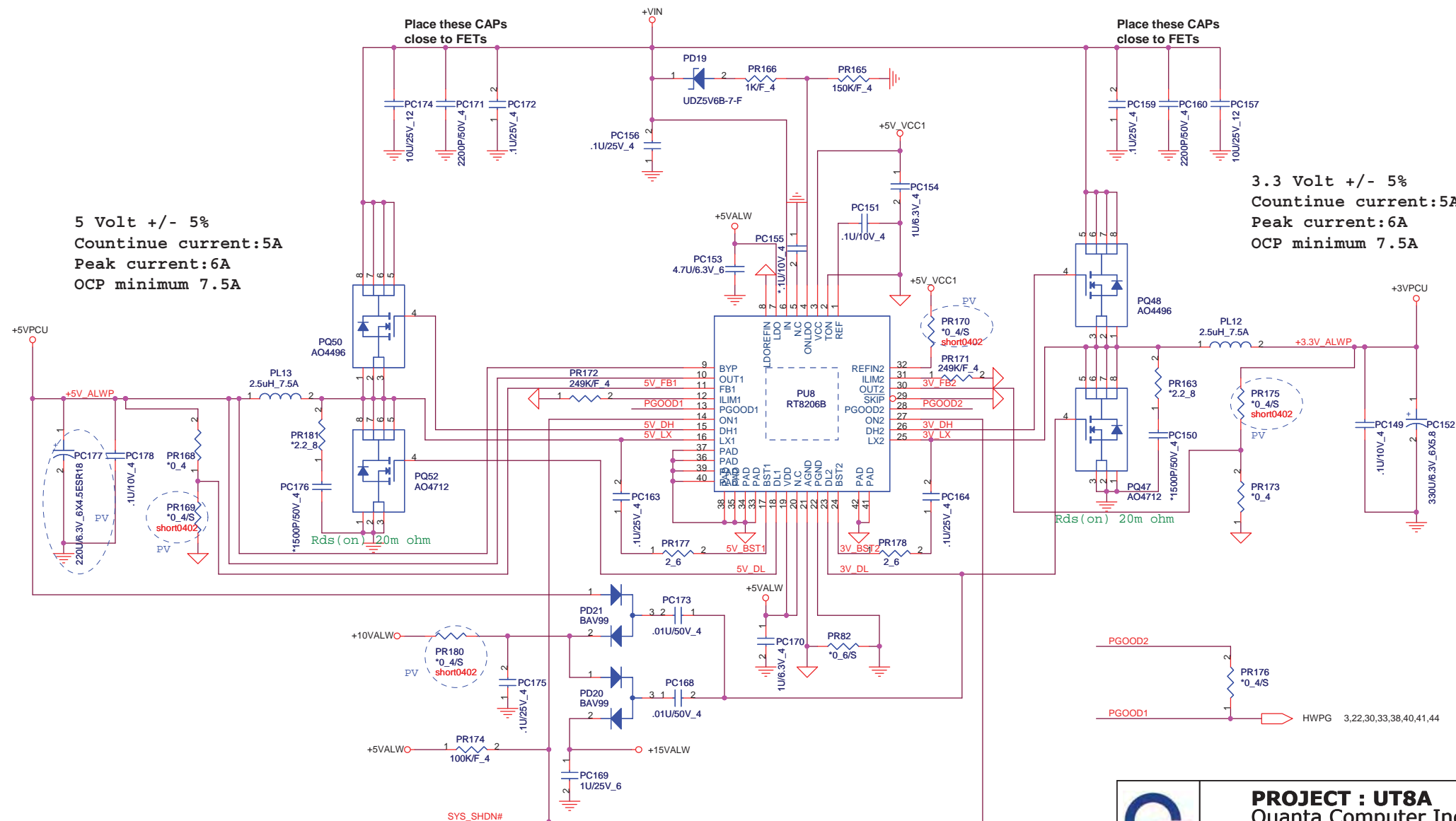
**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>CABLE DOCKING</b>	Rev 2A
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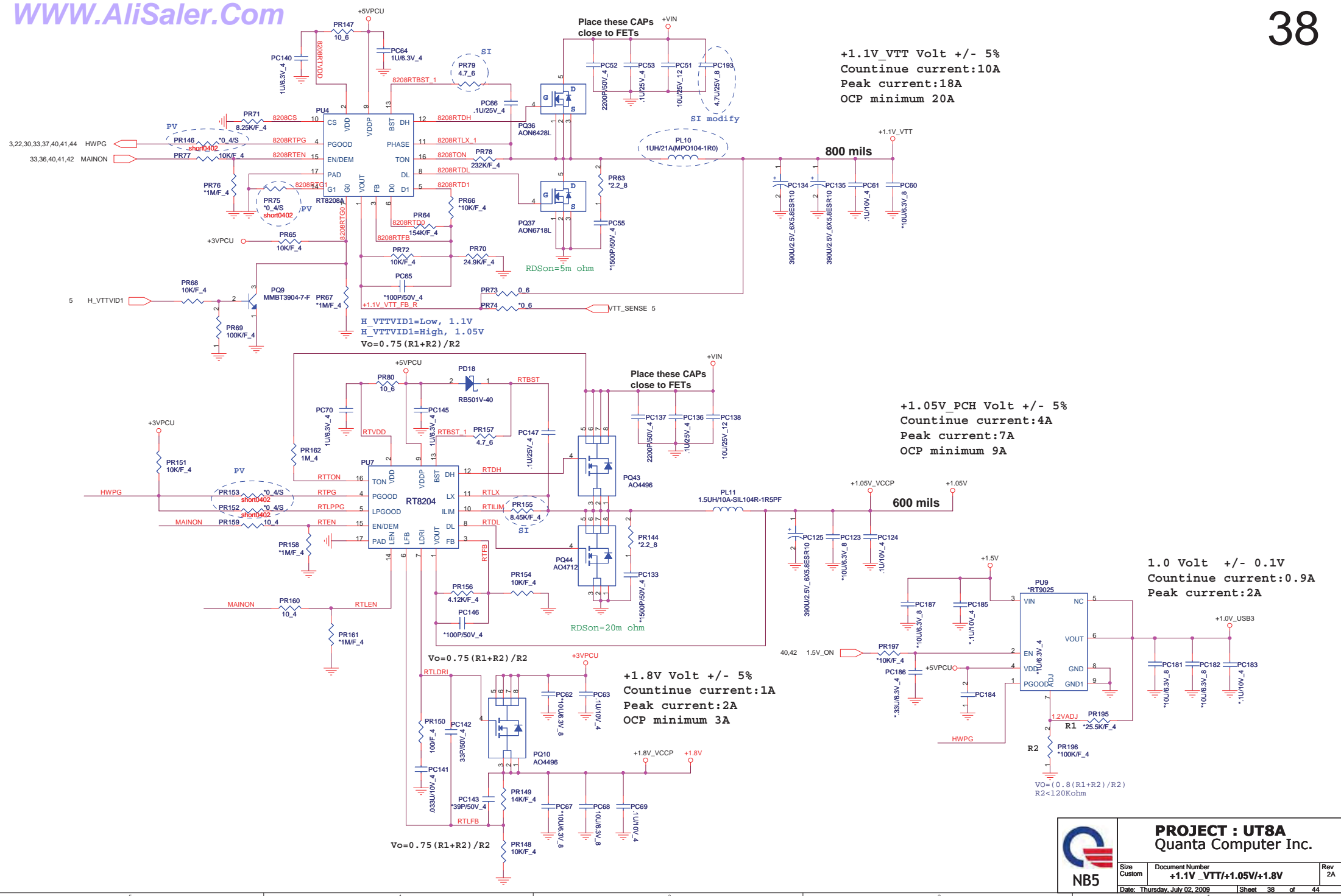


NB5

**PROJECT : UT8A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+5V/+3V (RT8206B)</b>	Rev 2A
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**PROJECT : UT8A**  
 Quanta Computer Inc.

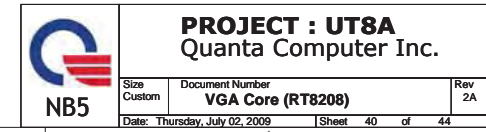
Size Custom	Document Number <b>+1.1V_VTT/+1.05V/+1.8V</b>	Rev 2A
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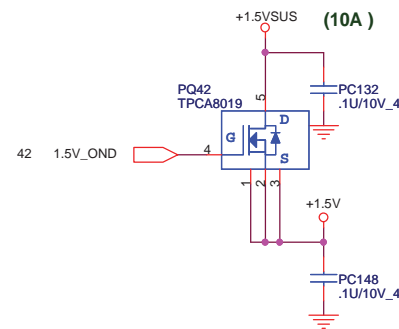
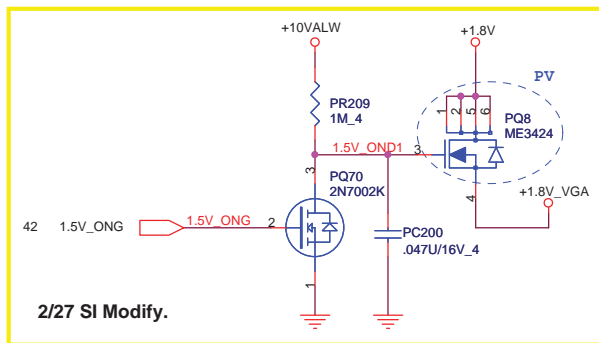
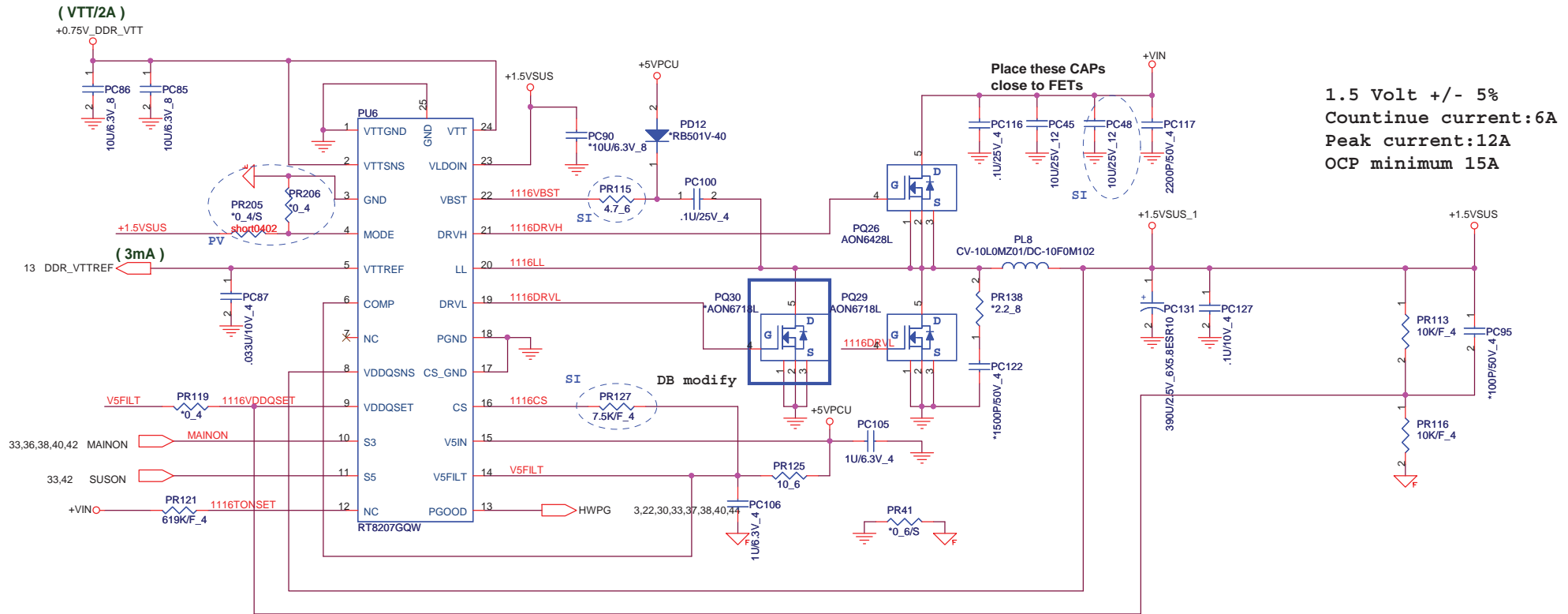




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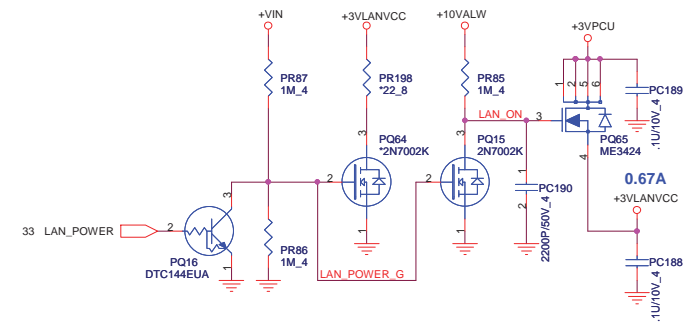




**PROJECT : UT8A**  
Quanta Computer Inc.

Size B	Document Number	Rev
	<b>+1.5VSUS DDR3 (RT8207)</b>	2A
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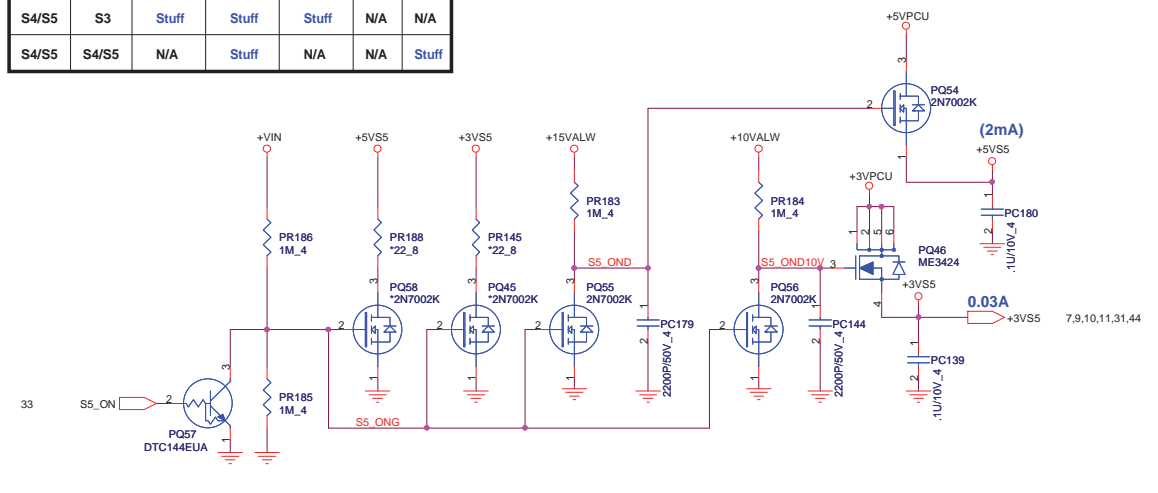




The schematic shows the power supply circuitry. It includes three input rails: +VIN, +1.5V, and +10VALW. The +VIN rail passes through resistor PR52 (1M\_4) to a node labeled 1.5V\_ONG. The +1.5V rail passes through resistor PR143 (22\_8) to a node labeled 1.5V\_ONG. The +10VALW rail passes through resistor PR60 (1M\_4) to a node labeled 1.5V\_OND. A 1.5V\_ON signal is shown entering the circuit from the left, passing through resistor PR42 (1M\_4) to the same 1.5V\_ONG node. This node is connected to the base of transistor PQ6 (DTC144EUA). The emitter of PQ6 is grounded. The collector of PQ6 is connected to the base of transistor PQ41 (2N7002K), which has its emitter grounded. The drain of PQ41 is connected to the base of transistor PQ7 (2N7002K), which also has its emitter grounded. The drain of PQ7 is connected to a capacitor PC41 (.01U/50V\_4) and a node labeled 1.5V\_ONG. A 38.40V source is connected to the gate of PQ6.



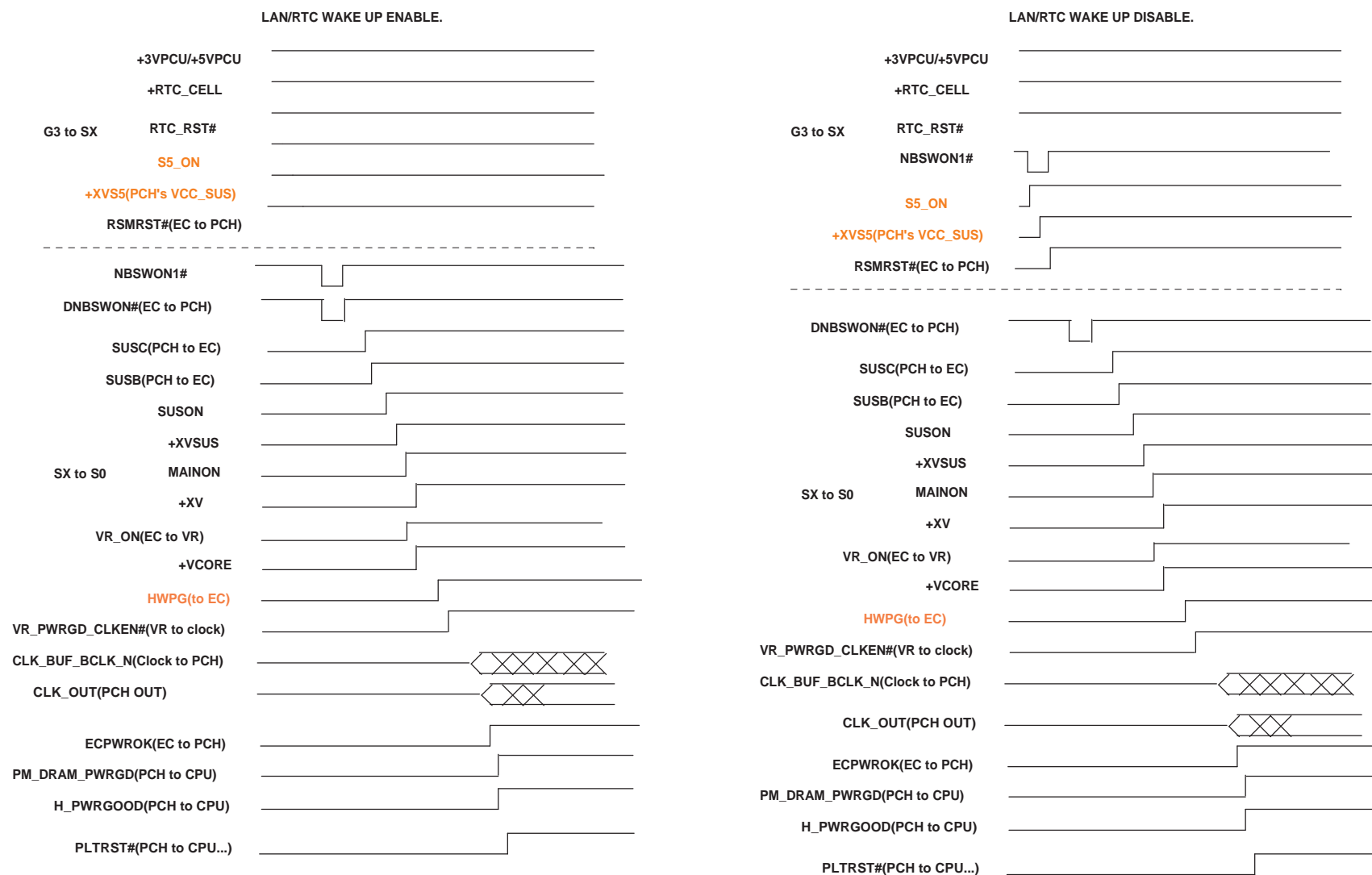
**f** Default



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## Power up sequence



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Date Thursday, July 02, 2009		Sheet 44 of 44